EE719 Mixed Signal VLSI Design

Course Project : Design of 8-bit Binary Current Steering DAC

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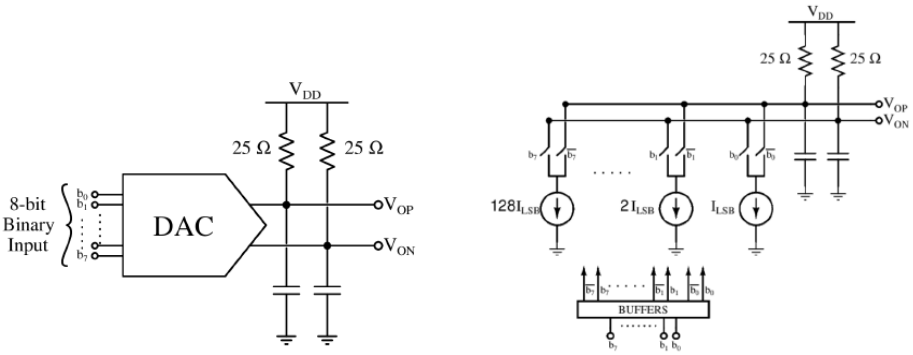
Contents

1 Target Specifications



(a) 8-bit DAC: top-level

(b) 8-bit DAC: circuit diagram

Figure 1: Overview of 8-bit DAC Architecture

Parameter	**Value**
Number of bits	8
Analog Supply Voltage (AV_{DD})	1.2/1.8 V
Digital Supply Voltage (DV_{DD})	1.2 V
Output Voltage Swing (Differential Peak-Peak), V_{FS}	> 0.8 V
INL	< 0.5 LSB
DNL	< 1 LSB
SFDR (Nyquist Bandwidth)	> 50 dB
Sampling Frequency (F_s)	1 GSps

Table 1: 8-bit DAC Specification

2 Design of unit cell of the 8 bit Binary DAC

2.1 Design procedure for unit cell

Parameter	Value
$\mu_n C_{ox}$	210 $\mu A/V^2$
$\mu_p C_{ox}$	140 $\mu A/V^2$
A_β	2% μm
$A_{V_{TH}}$	2.3 $mV.\mu m$

Table 2: Given MOS Device parameter values

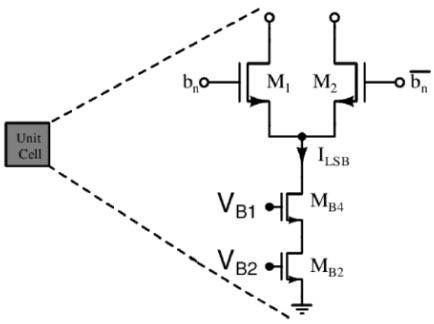


Figure 2: Schematic of DAC unit cell

2.1.1 Determining I_{LSB} and V_{FS}

From the circuit diagram shown in figure 31 (b) we can conclude

$$\begin{aligned} V_{OP,max} &= V_{DD} \\ V_{ON,min} &= V_{DD} - 255 \times I_{LSB} \times R \\ \implies V_{out,max} &= V_{OP,max} - V_{ON,min} = 255 \times I_{LSB} \times R \\ V_{OP,min} &= V_{DD} - 255 \times I_{LSB} \times R \\ V_{ON,max} &= V_{DD} \\ \implies V_{out,min} &= V_{OP,min} - V_{ON,max} = -255 \times I_{LSB} \times R \end{aligned}$$

$\implies V_{FS} = V_{out,max} - V_{out,min} = 510 \times I_{LSB} \times R = 510 \times 25 \times I_{LSB} = 12750 \times I_{LSB}$

We want $V_{FS} > 0.8\ V$.

$$\implies 12750 \times I_{LSB} > 0.8$$

$$I_{LSB} > \frac{0.8}{12750} = 62.75\ \mu A \tag{1}$$

For high output impedance, the differential-pair transistors (M_1 and M_2) must operate in saturation.

$$\implies V_{D_{M_{1,2}}} > V_{G_{M_{1,2}}} - V_{TN} > V_{S_{M_{1,2}}} \tag{2}$$

Assuming $AV_{DD} = DV_{DD} = 1.2\ V$, in the worst case we want

$$V_{DD} - 255 \times I_{LSB} \times R > V_{DD} - V_{TN}$$
$$\implies I_{LSB} < \frac{V_{TN}}{255 \times 25}$$

Assuming $V_{TN} \approx 500\ mV$

$$I_{LSB} < \frac{0.5}{255 \times 25} = 78.43\ \mu A \tag{3}$$

From (1) and (3),

$$62.75\ \mu A < I_{LSB} < 78.43\ \mu A$$

Let,

$$\mathbf{I_{LSB} = 70\ \mu A} \tag{4}$$

$$\implies \mathbf{V_{FS} = 12750 \times 70 \times 10^{-6} = 0.8925\ V \approx 0.9\ V} \tag{5}$$

2.1.2 Determining aspect ratios of M_{B2} and M_{B4}

From equation (2),

$$V_{S_{M_{1,2}}} < 1.2 - 0.5 = 0.7\ V \tag{6}$$

For both the biasing transistors to operate in saturation,

$$V_{D_{M_{B2}}} > V_{DSAT_{M_{B2}}} \tag{7}$$
$$V_{S_{M_{1,2}}} > V_{D_{M_{B2}}} + V_{DSAT_{M_{B4}}} \tag{8}$$

Since both M_{B2} and M_{B4} have the same drain current and assuming they have the same aspect ratios

$$V_{DSAT_{M_{B2}}} = V_{DSAT_{M_{B4}}} = V_{DSAT_{M_B}} \text{(say)}$$

From (6), (7) and (8),

$$2 \times V_{DSAT_{M_B}} < 700\ mV \implies V_{DSAT_{M_B}} < 350\ mV$$

Let,

$$V_{DSAT_{M_B}} = 200\ mV$$
$$V_{D_{M_{B2}}} = 300\ mV$$
$$V_{B2} = V_{DSAT_{M_B}} + V_{TN} = 700\ mV \tag{9}$$
$$V_{B1} = V_{D_{M_{B2}}} + V_{DSAT_{M_B}} + V_{TN} = 1\ V \tag{10}$$

Now,

$$I_{LSB} = \frac{\mu_n C_{ox}}{2} \frac{W_B}{L_B} \left(V_{DSAT_{M_B}}\right)^2$$

$$\implies \frac{W_B}{L_B} = \frac{2I_{LSB}}{\mu_n C_{ox} \left(V_{DSAT_{M_B}}\right)^2} = \frac{2 \times 70}{210 \times 0.2^2} = \frac{50}{3}$$

Thus,

$$\frac{\mathbf{W_{M_{B2}}}}{\mathbf{L_{M_{B2}}}} = \frac{\mathbf{W_{M_{B4}}}}{\mathbf{L_{M_{B4}}}} = \frac{\mathbf{50}}{\mathbf{3}} \tag{11}$$

2.1.3 Determining aspect ratios of M_1 and M_2

From equations (6) and (8),

$$500\ mV < V_{S_{M_{1,2}}} < 700\ mV$$

Let,

$$V_{S_{M_{1,2}}} = 600\ mV$$

Both M_1 and M_2 will have same parameters. Depending on the input, one transistor will be off while other will be on with $I_{DS} = I_{LSB}$. Thus,

$$I_{LSB} = \frac{\mu_n C_{ox}}{2} \frac{W_{1,2}}{L_{1,2}} \left(V_{DD} - V_{S_{M_{1,2}}} - V_{TN}\right)^2$$

$$\implies \frac{W_{1,2}}{L_{1,2}} = \frac{2I_{LSB}}{\mu_n C_{ox} \left(V_{DD} - V_{S_{M_{1,2}}} - V_{TN}\right)^2} = \frac{2 \times 70}{210 \times (1.2 - 0.6 - 0.5)^2} = \frac{200}{3}$$

Thus,

$$\frac{\mathbf{W_{M_1}}}{\mathbf{L_{M_1}}} = \frac{\mathbf{W_{M_2}}}{\mathbf{L_{M_2}}} = \frac{\mathbf{200}}{\mathbf{3}} \tag{12}$$

2.1.4 Determining W and L for all transistors

For a current-steering binary DAC,

$$INL_{max} = \frac{\sigma_{I_{LSB}}}{2I_{LSB}} \sqrt{2^N}\ LSB \tag{13}$$

$$DNL_{max} = \frac{\sigma_{I_{LSB}}}{I_{LSB}} \sqrt{2^N}\ LSB \tag{14}$$

From Pelgorm's equations for matching properties of MOS transistors we know,

$$\frac{\sigma_{I_d}^2}{I_d^2} = \frac{4\sigma_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_\beta^2}{\beta^2} \tag{15}$$

$$\sigma_{V_{TH}}^2 \approx \frac{A_{V_{TH}}^2}{WL} \tag{16}$$

$$\frac{\sigma_\beta^2}{\beta^2} \approx \frac{A_\beta^2}{WL} \tag{17}$$

$$\implies \frac{\sigma_{I_{LSB}}}{I_{LSB}} = \sqrt{\frac{4A_{V_{TH}}^2}{W_B L_B (V_{DSAT_{M_B}})^2} + \frac{A_\beta^2}{W_B L_B}} \tag{18}$$

As per the given specs, we want $INL_{max} < 0.5\ LSB$ and $DNL_{max} < 1\ LSB$

$$\frac{\sigma_{I_{LSB}}}{I_{LSB}}\sqrt{2^8} < 1 \implies \frac{\sigma_{I_{LSB}}}{I_{LSB}} < 0.0625$$

From equation (18),

$$\implies \sqrt{\frac{4A_{V_{TH}}^2}{W_B L_B (V_{DSAT_{M_B}})^2} + \frac{A_\beta^2}{W_B L_B}} < 0.0625$$

$$\implies W_B L_B > 256 \times \left(\frac{4A_{V_{TH}}^2}{(V_{DSAT_{M_B}})^2} + A_\beta^2 \right)$$

Substituting all values,

$$W_B L_B > 256 \times \left(\frac{4 \times 2.3^2}{(200)^2} + 0.02^2 \right) = 0.2378\ \mu m^2 \tag{19}$$

From (11) and (19),

$$\frac{50}{3} L_B^2 > 0.2378\ \mu m^2 \implies L_B > 0.119\ \mu m$$

Let,

$$\mathbf{L_{M_{B2}} = L_{M_{B4}} = L_B = 140\ nm} \tag{20}$$

$$\mathbf{W_{M_{B2}} = W_{M_{B4}} = W_B = \frac{50}{3} \times L_B = 2.3\ \mu m} \tag{21}$$

To ensure fast switching and minimal capacitance at the tail node, the switching transistors are designed with the minimum channel length. Using equation (9),

$$\mathbf{L_{M_1} = L_{M_2} = L_{1,2} = 45\ nm} \tag{22}$$

$$\mathbf{W_{M_1} = W_{M_2} = W_{1,2} = \frac{200}{3} \times L_{1,2} = 3\ \mu m} \tag{23}$$

Parameters	$\mathbf{M_{B2}}$	$\mathbf{M_{B4}}$	$\mathbf{M_1}$	$\mathbf{M_2}$	$\mathbf{V_{FS}}$	$\mathbf{I_{LSB}}$
Width	2.3 μm	2.3 μm	3 μm	3 μm	0.9 V	70 μA
Length	140 nm	140 nm	45 nm	45 nm	-	-

Table 3: Chosen parameter values for unit cell

2.2 Cascode current source bias

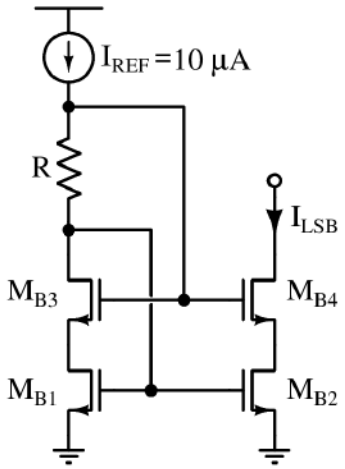


Figure 3: Cascode Current Source Bias

$$\frac{I_{LSB}}{I_{ref}} = \frac{70}{10} = 7$$

$$\implies \frac{W_{M_{B2}}}{L_{M_{B2}}} = \frac{W_{M_{B4}}}{L_{M_{B4}}} = 7\frac{W_{M_{B1}}}{L_{M_{B1}}} = 7\frac{W_{M_{B3}}}{L_{M_{B3}}}$$

Assuming same lengths of all transistors for better matching, from equation (20) and (21),

$$\mathbf{L_{M_{B1}} = L_{M_{B2}} = 140\ nm} \tag{24}$$

$$\mathbf{W_{M_{B1}} = W_{M_{B3}} = \frac{2.3}{7} = 0.329\ \mu m \approx 330\ nm} \tag{25}$$

From equation (9) and (10),

$$V_{B1} - V_{B2} = 300\ mV = I_{REF} \times R$$

$$\mathbf{R = \frac{0.3}{10 \times 10^{-6}} = 30\ k\Omega} \tag{26}$$

Parameter	$\mathbf{M_{B1}}$	$\mathbf{M_{B3}}$	**R**
Width	330 nm	330 nm	30 $k\Omega$
Length	140 nm	140 nm	-

Table 4: Chosen parameter values for cascode current source

2.3 Tapered buffer

For a tapered buffer with constant stage ratio ρ and N stages,

$$\rho = \left(\frac{C_L}{C_{in}}\right)^N$$

Total delay is minimised when $\rho = e$.

$$N = \left\lfloor ln\left(\frac{C_L}{C_{in}}\right)\right\rfloor$$

Assuming $C \propto W \times L$, considering C_{in} of minimum sized inverter and C_L of switching transistors of unit cell,

$$N = \left\lfloor ln\left(\frac{3000 \times 45}{200 \times 45 + 120 \times 45}\right)\right\rfloor = \lfloor 2.238 \rfloor = 2$$

Thus, required number of stages in the buffer is **2**

3 Circuit implementation of DAC unit cell on Cadence

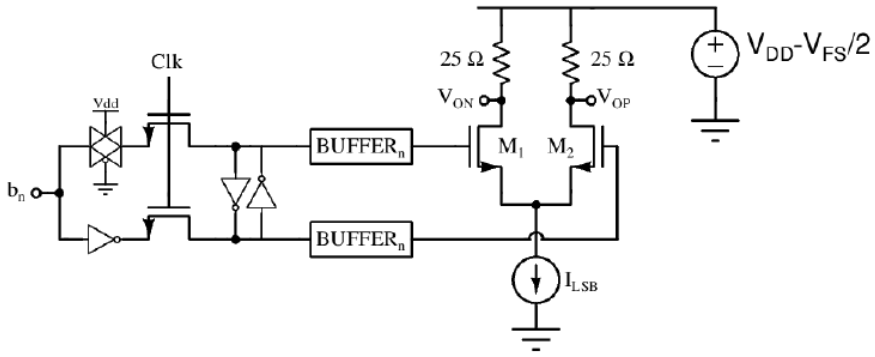


Figure 4: DAC unit cell with resistive load

3.1 Unit cell implementation

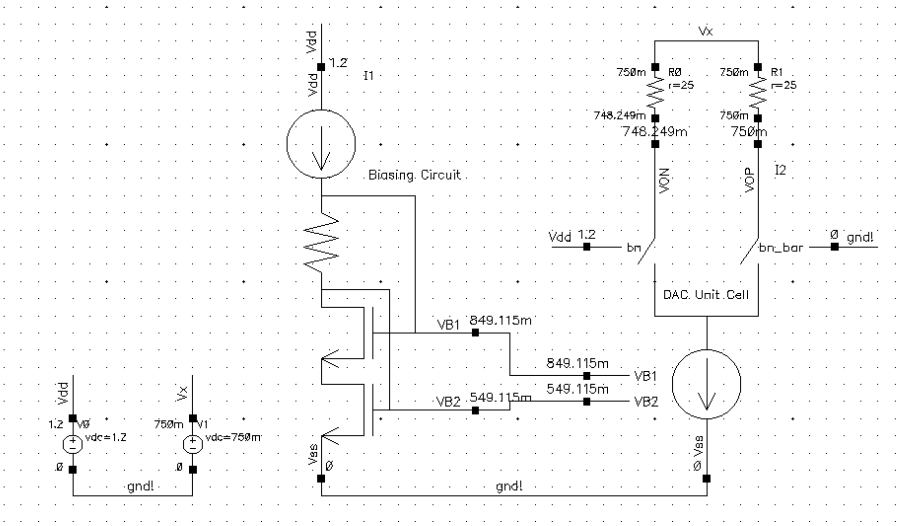
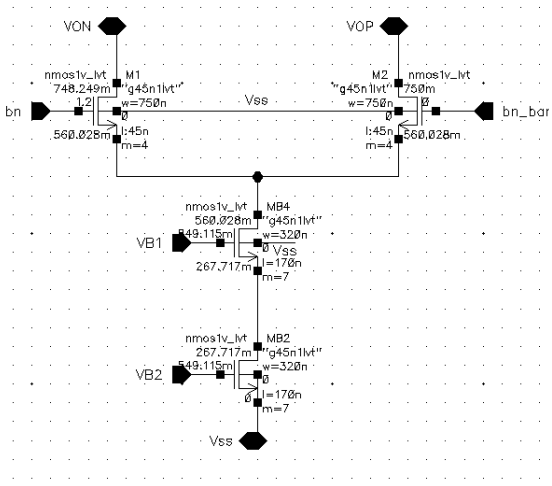
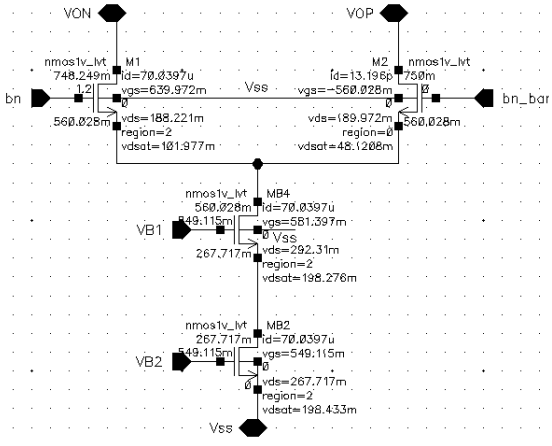


Figure 5: DAC unit cell with current source biasing



(a) Component Parameters

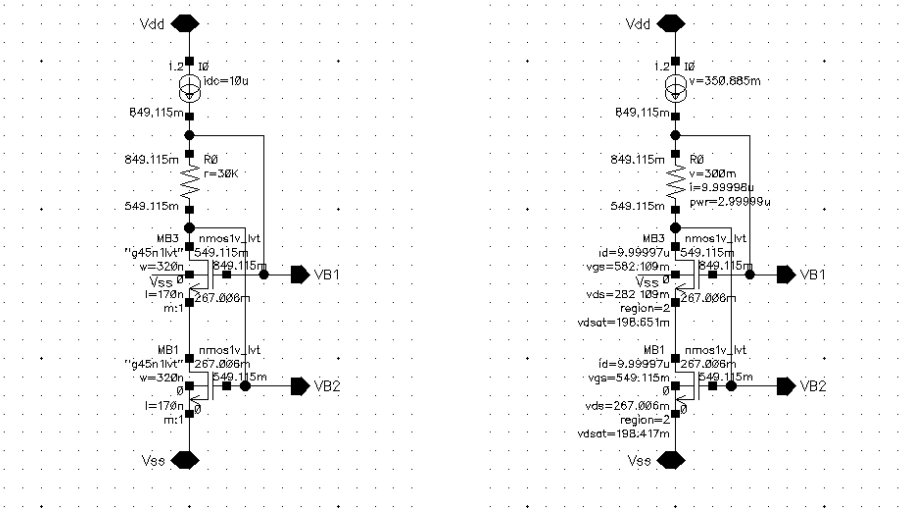


(b) DC Operating Points

Figure 6: DAC Unit Cell

Parameters	$\mathbf{M_{B2}}$	$\mathbf{M_{B4}}$	$\mathbf{M_1}$	$\mathbf{M_2}$
Width	2.24 μm	2.24 μm	3 μm	3 μm
Length	170 nm	170 nm	45 nm	45 nm

Table 5: Chosen parameter values for unit cell



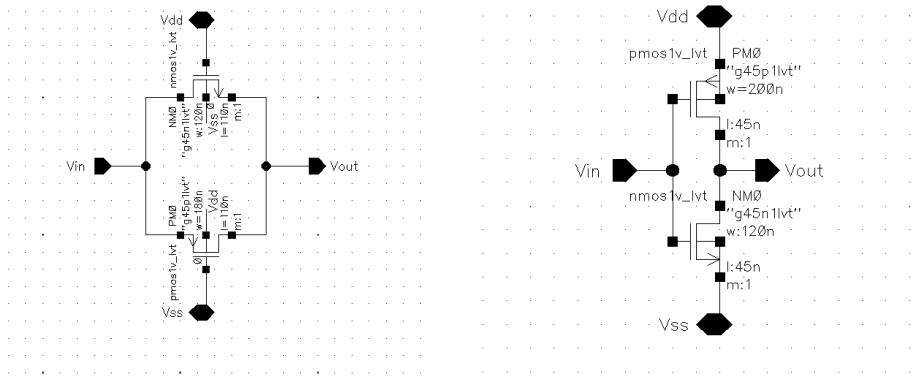
(a) Component Parameters (b) DC Operating Points

Figure 7: Current Source Biasing

Parameter	M_{B1}	M_{B3}	R
Width	320 nm	320 nm	30 $k\Omega$
Length	170 nm	170 nm	-

Table 6: Chosen parameter values for cascode current source

3.2 Pass transistor



(a) Pass transistor (b) Minimum Sized Inverter

Figure 8: Component Parameters of pass transistor and inverter

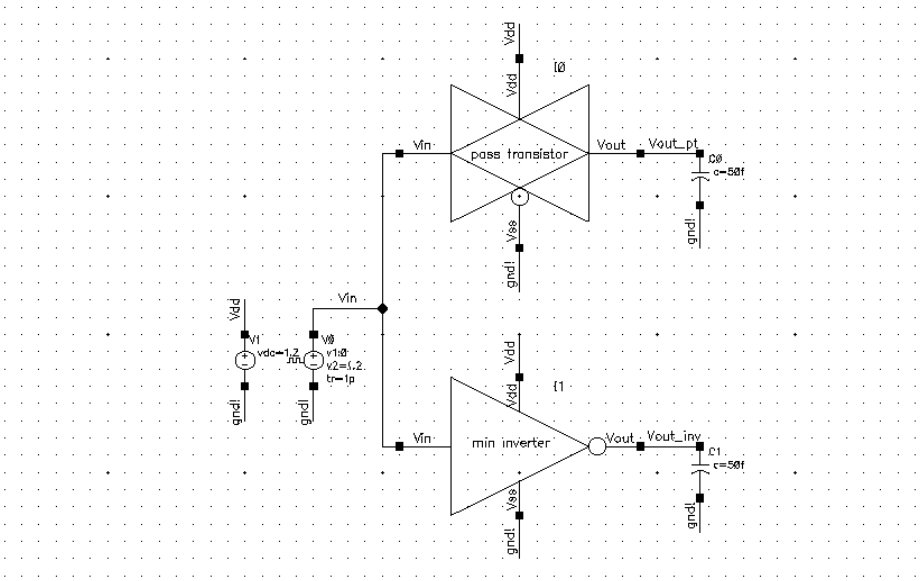


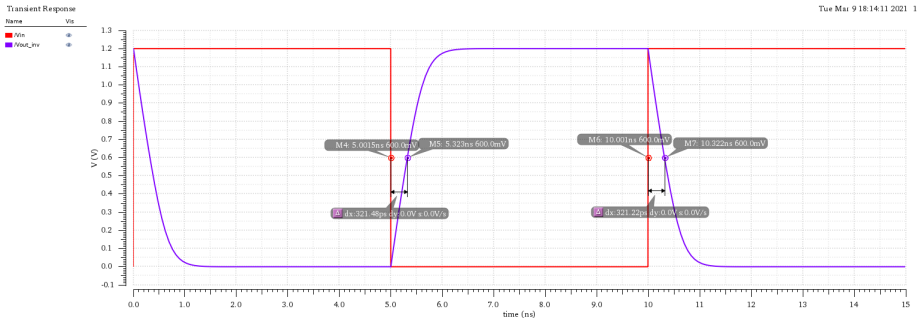
Figure 9: Pass transistor and Inverter delay comparison testbench

Parameter	$\mathbf{M_N}$	$\mathbf{M_P}$
Width	120 nm	200 nm
Length	45 nm	45 nm

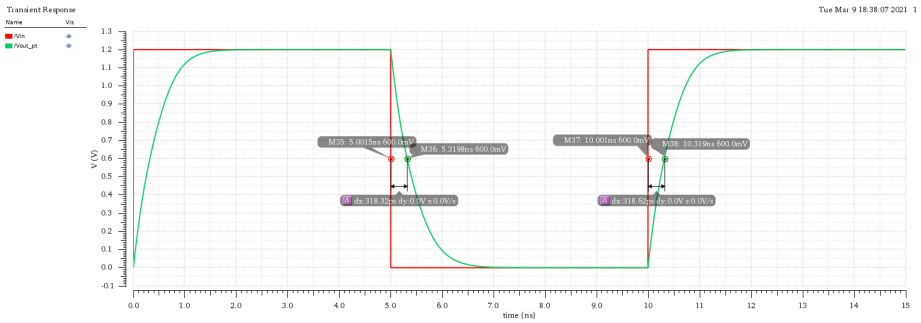
Table 7: Chosen parameter values for minimum sized inverter

Parameter	$\mathbf{M_N}$	$\mathbf{M_P}$
Width	120 nm	180 nm
Length	110 nm	110 nm

Table 8: Chosen parameter values for pass transistor



(a) Inverter Delay



(b) Pass transistor delay

Figure 10: Pass transistor and Inverter transient analysis

Delay	Inverter	Pass Transistor
Low-High	321.22 ps	318.62 ps
High-Low	321.48 ps	318.32 ps

Table 9: Pass transistor and Inverter delay comparison

The delay for both inverter and pass transistor is approximately same and equal to **320 ps**.

3.3 Digital buffer

From previous analysis we know that number of inverter stages in buffer is 2. Also, the gate capacitance to be driven by buffer (C_{gg} of M_1 or M_2) is approximately 2.26 fF.

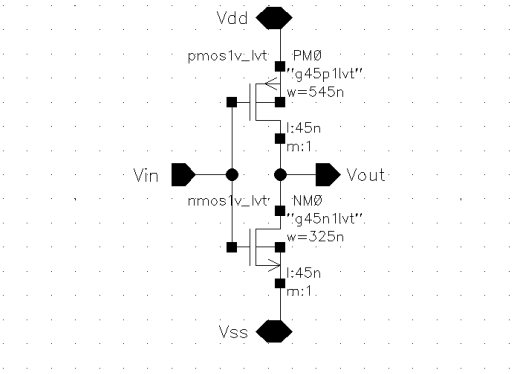


Figure 11: Scaled Inverter

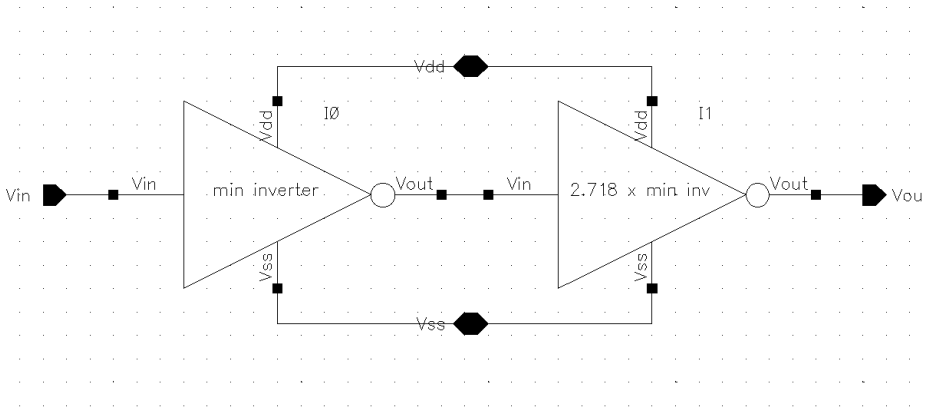


Figure 12: Buffer schematic

Size of minimum sized inverter are given in Table 4. Size of scaled inverter are given in Table 7.

Parameter	$\mathbf{M_N}$	$\mathbf{M_P}$
Width	545 nm	325 nm
Length	45 nm	45 nm

Table 10: Chosen parameter values for 2.718x scaled inverter

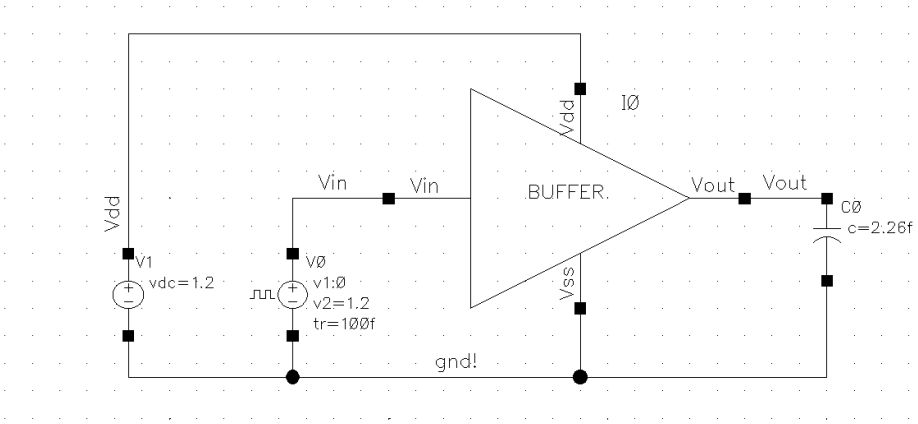


Figure 13: Buffer testbench

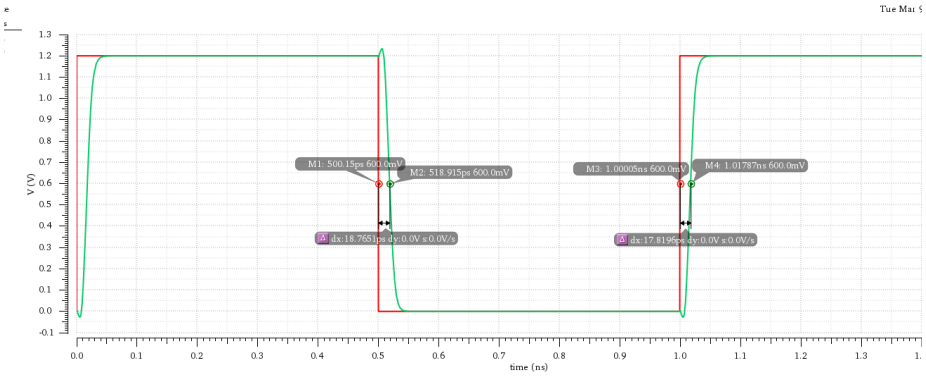


Figure 14: Buffer transient analysis

	Buffer Delay
Low-High	17.82 ps
High-Low	18.77 ps

Table 11: Buffer delay

3.4 Analysis of unit cell

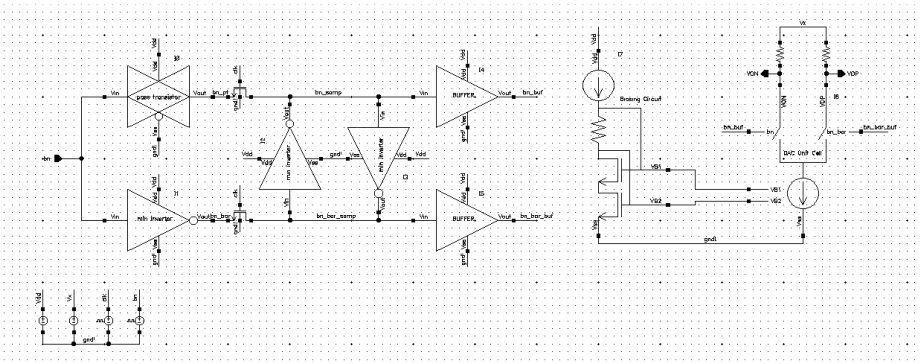
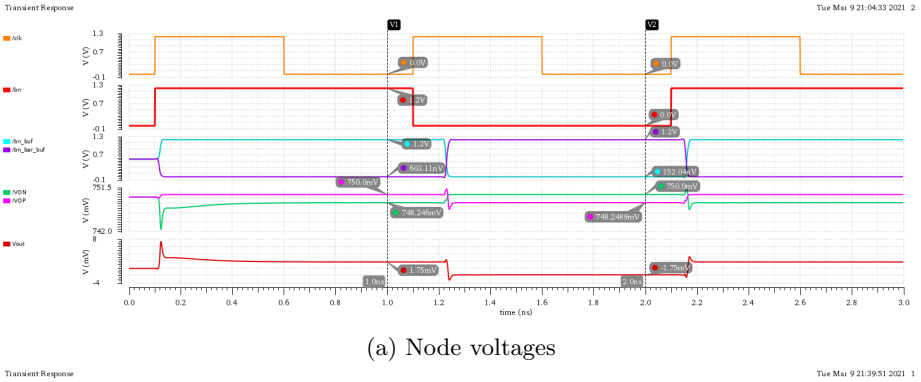
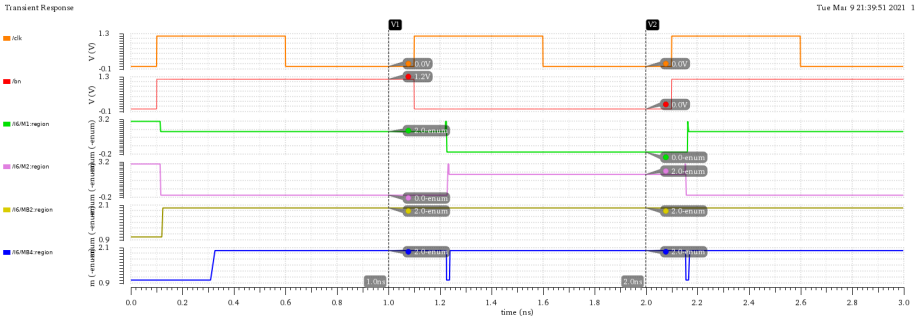


Figure 15: Complete testbench for DAC unit cell



(a) Node voltages



(b) Region of operation of transistors in unit cell

Figure 16: Transient Analysis with varying b_n

From Figure 14, $V_{out} = V_{OP} - V_{ON}$ is 1.75 mV when $b_n = 1$ and -1.75 mV when $b_n = 0$. This is what we expect because $I_{LSB} \times R = 70 \times 25 = 1750\ \mu V = 1.75\ mV$.

The cross point of input signals has an impact on circuit performance. We see transistor M_{B4} enters subthreshold region for some time during the cross over. This changes the output impedance of the tail current source, thus causing dynamic errors. Since transitions happen quickly, at high frequency the parasitic capacitances provide a low impedance path to signals, thus causing distortion in the output. Therefore, the spurious free dynamic range (SFDR) will be affected.

4 8-bit DAC implementation and characterization

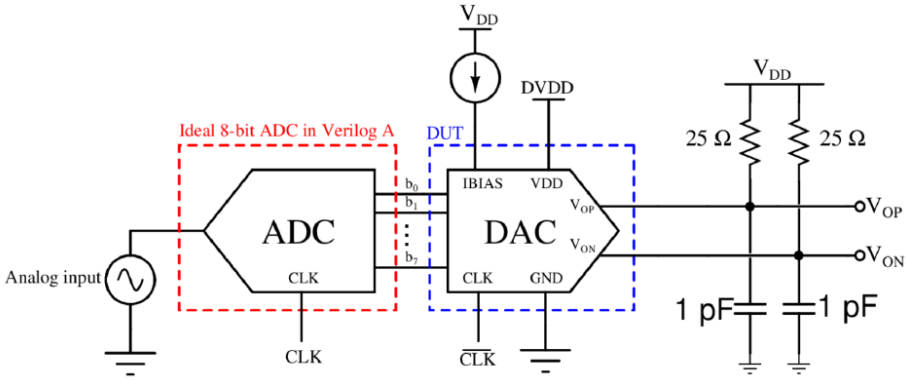


Figure 17: DAC unit cell with resistive load

4.1 8-bit DAC implementation

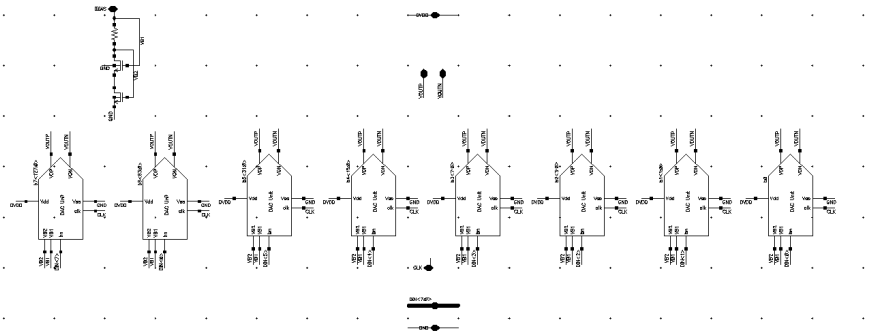


Figure 18: 8-bit DAC schematic

4.2 Transient analysis with Ramp input

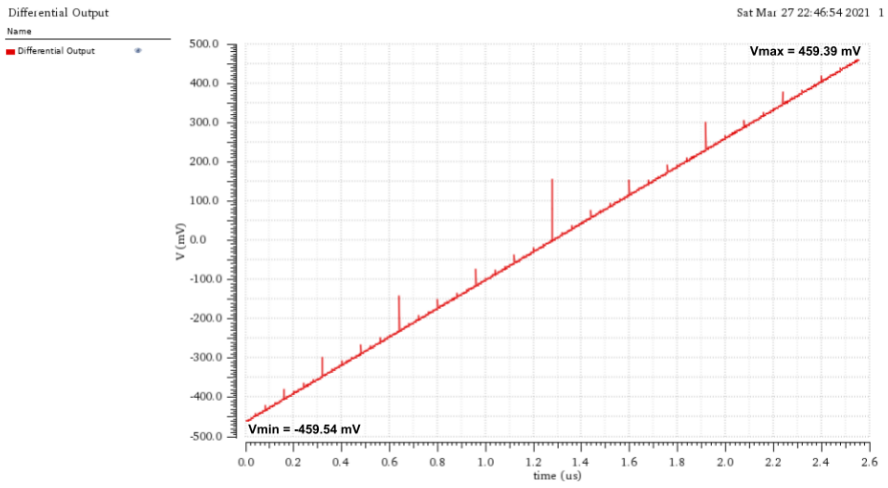


Figure 19: Differential output with ramp input

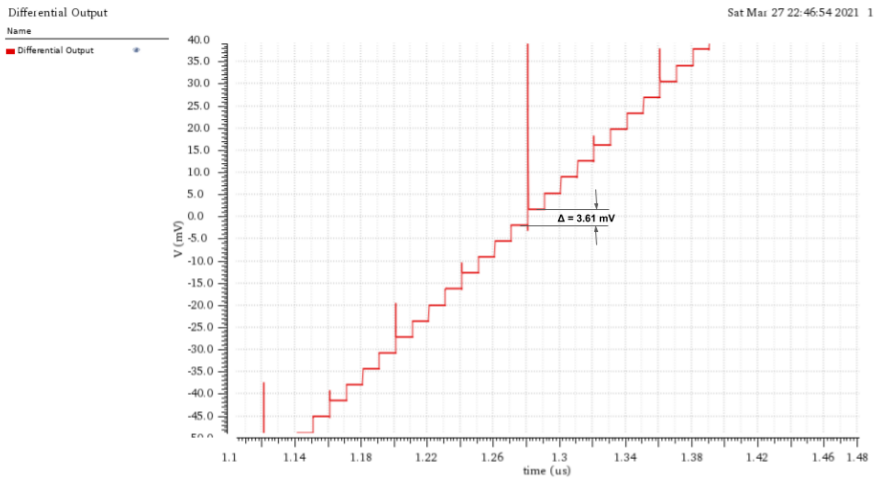


Figure 20: Zoomed in differential output with ramp input

Observations:

1. We see a staircase output waveform as expected
2. The glitches are most significant during MSB transitions
3. $V_{min} = -459.54\ mV$
4. $V_{max} = 459.39\ mV$
5. $V_{lsb} = 3.61\ mV$

4.3 Errors and non-linearities

Since I had designed for $V_{FS} = 0.9\ V$, $V_{min,ideal} = -450\ mV$ and $V_{max,ideal} = 450mV$. The values for offset, full scale and gain error have been calculated accordingly.

Offset Error	Full Scale Error	Relative Gain Error
-9.54 mV	9.39 mV	1.021

Table 12: DAC errors

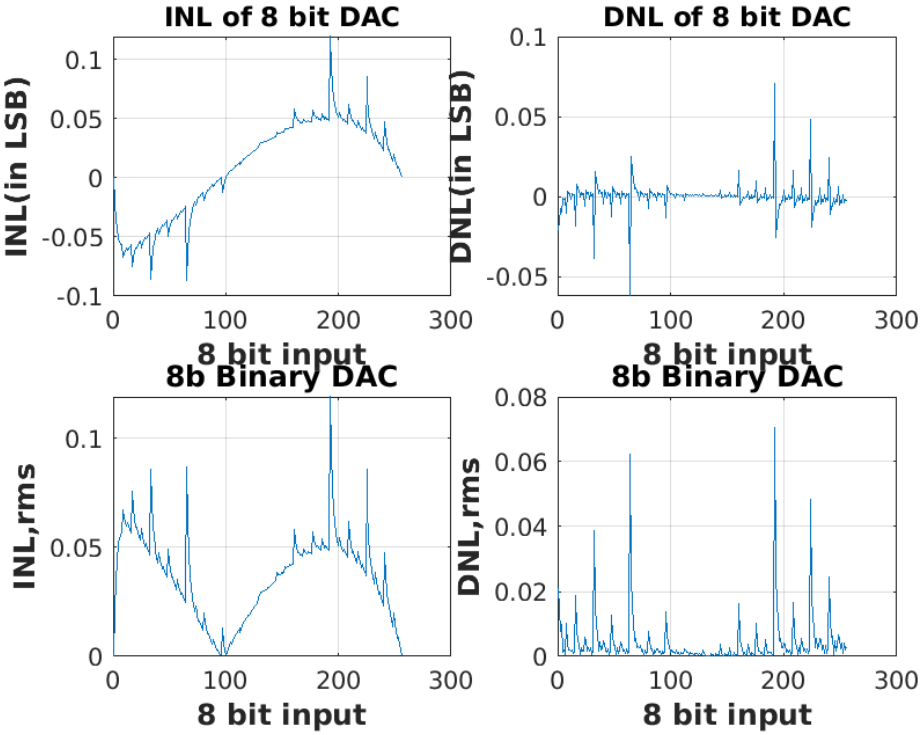


Figure 21: INL and DNL of output obtained with single run

1. Maximum $INL_{rms} = 0.12\ LSB$
2. Maximum $DNL_{rms} = 0.07\ LSB$

Observe that the specification of $INL < 0.5\ LSB$ and $DNL < 1\ LSB$ are met.

4.4 Monte Carlo analysis

To speed up the Monte Carlo simulations, the ramp slope was increased and transient simulation duration was reduced to 256 ns as per instructions.

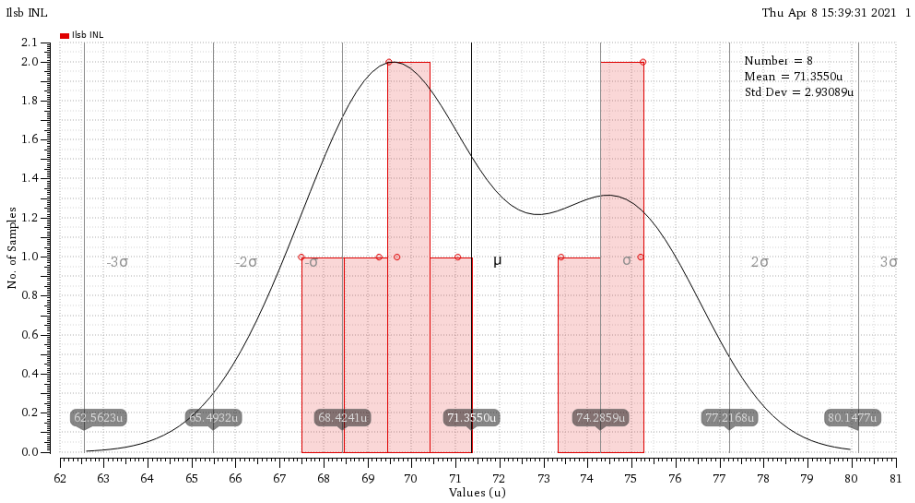


Figure 22: I_{LSB} variation

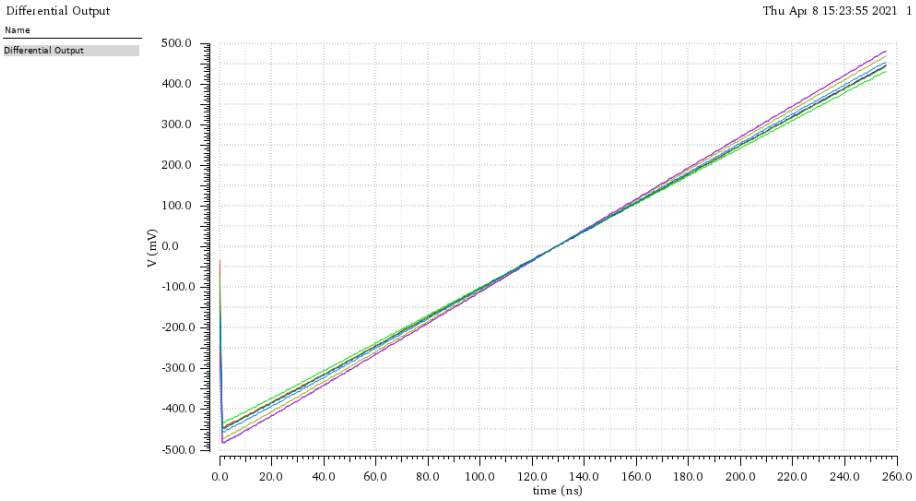


Figure 23: Output variation

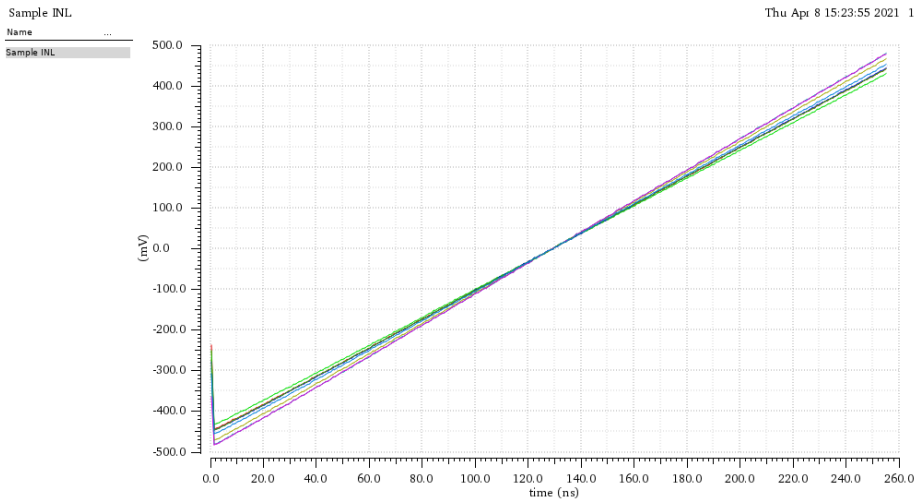


Figure 24: Sample INL

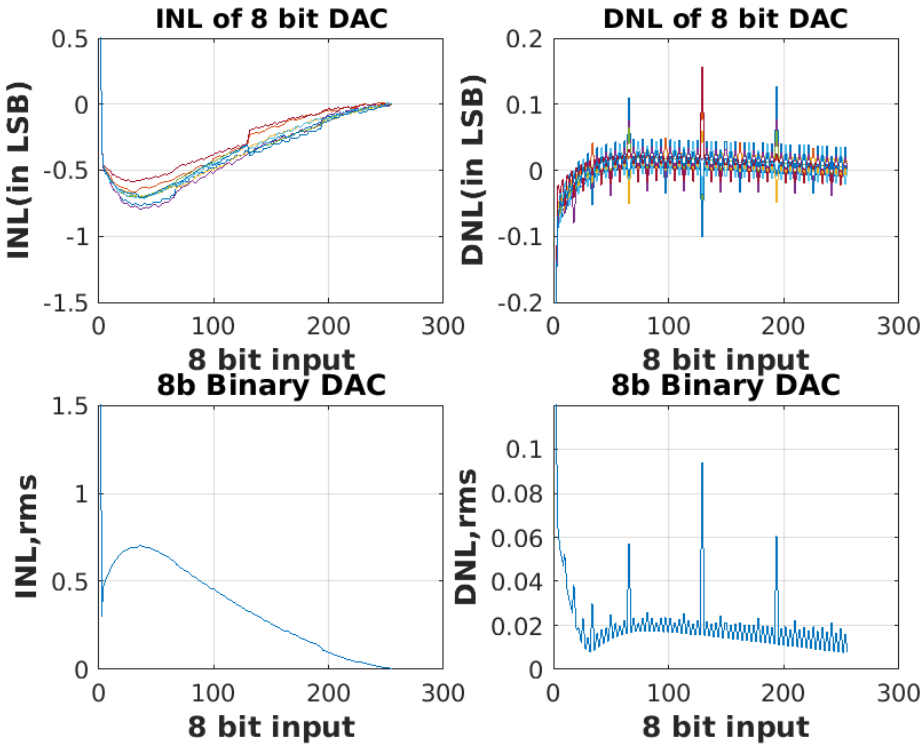


Figure 25: INL and DNL of output obtained with 8 point Monte Carlo Simulation

1. Maximum $INL_{rms} = 0.7\ LSB$
2. Maximum $DNL_{rms} = 0.1\ LSB$

The first output point from the simulation result isn't accurate and therefore the spike at first transition should be ignored when looking at DNL and INL plots. Observe that DNL specification is met while INL is slightly higher than desired.

4.5 FFT analysis with low frequency input

$$f_{sig} = \frac{199}{2048} \times 1\ GHz = 97.65\ MHz$$

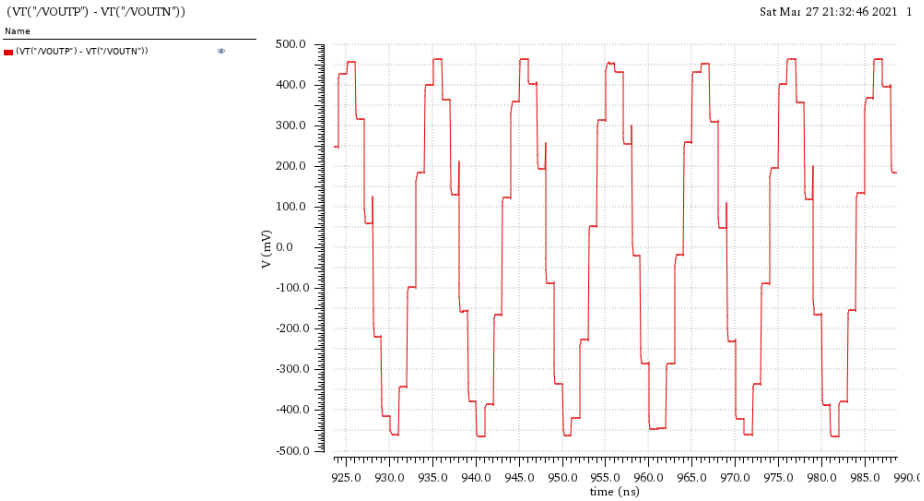


Figure 26: Transient Waveform

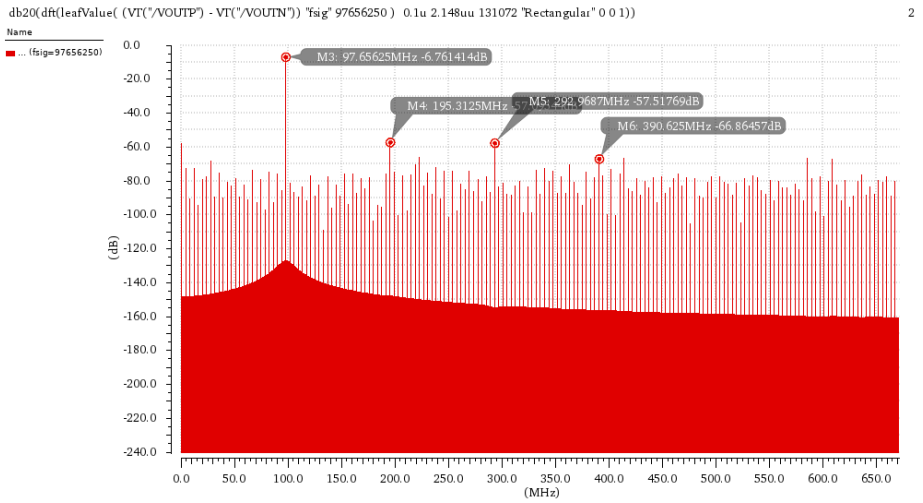


Figure 27: FFT

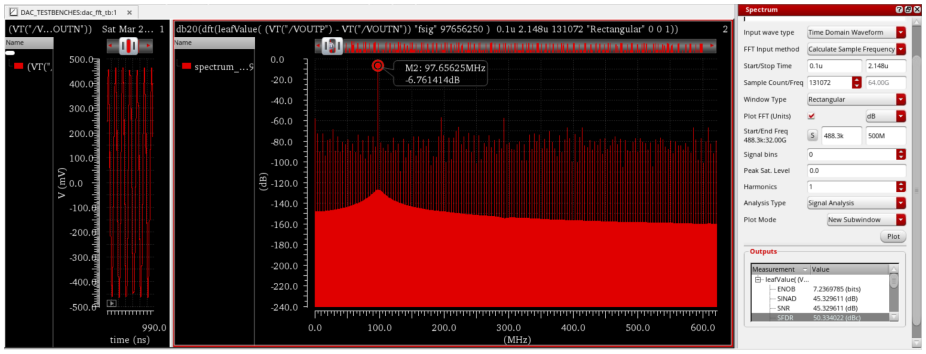


Figure 28: All results

The harmonics are due to capacitive coupling which causes distortion during transitions. To improve the SNDR we need to minimize the capacitance at the drain of cascode current source in unit cell.

4.6 FFT analysis with near Nyquist frequency input

$$f_{sig} = \frac{999}{2048} \times 1\ GHz = 488.28\ MHz$$

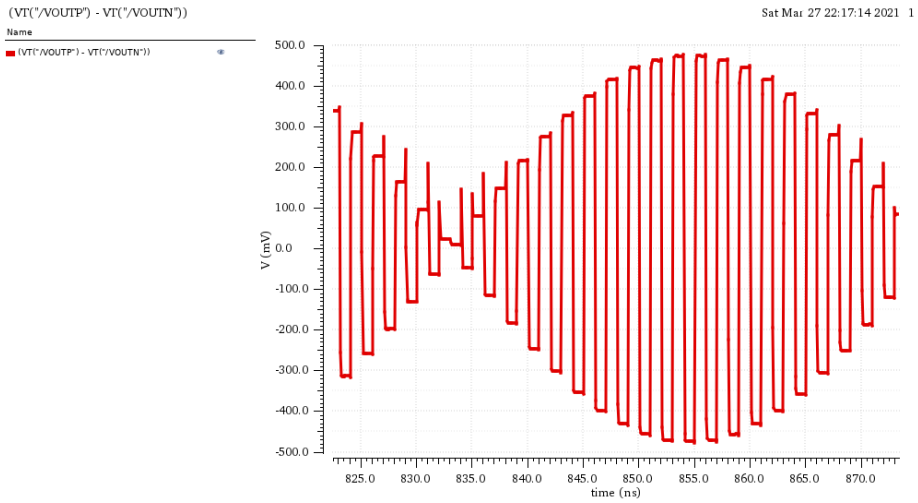


Figure 29: Transient Waveform

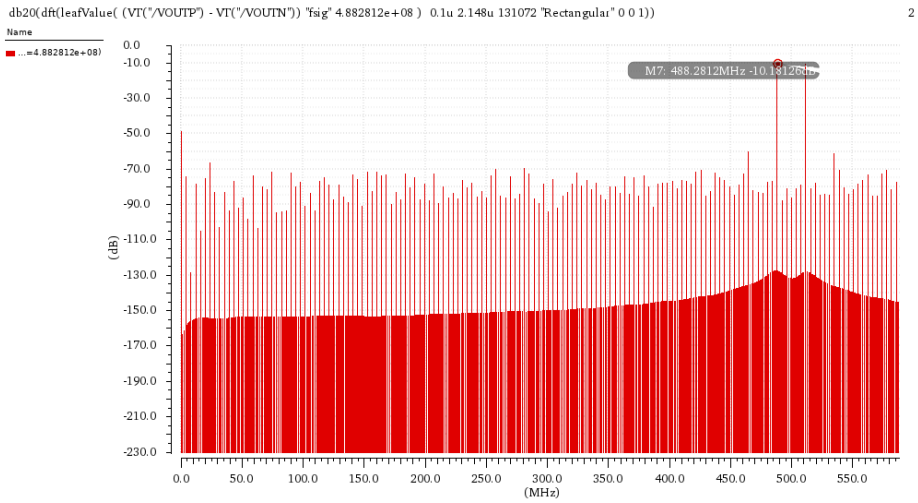


Figure 30: FFT

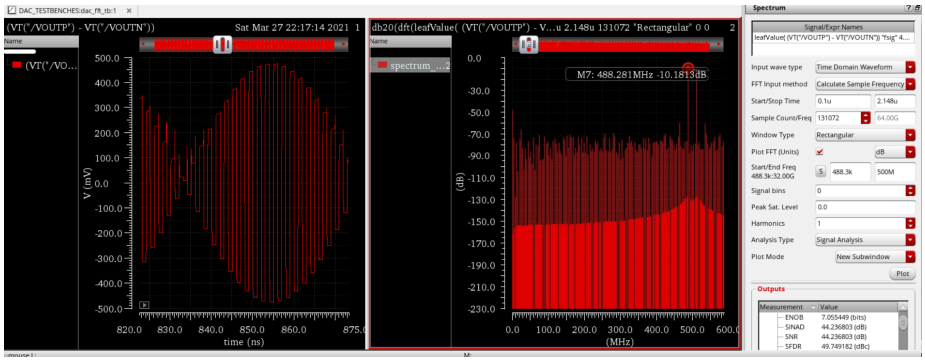


Figure 31: All results

There are no harmonics here since the signal frequency is close to Nyquist frequency, so only the fundamental tone lies within the band.

4.7 Dynamic performance

	SFDR	**SNDR**	**ENOB**
$f = 97.65\ MHz$	50.33 dB	45.33 dB	7.24 bits
$f = 488.28\ MHz$	49.75 dB	44.24 dB	7.06 bits

Table 13: Dynamic Performance Characteristics

4.8 Power analysis

Theoretically, total static power consumed $= V_{DD} \times I_{LSB} \times 255 \approx 22\ mW$

From simulation with ramp input,
Average power consumed by analog part = **22.23 mW**. This matches the theoretical calculation.
Average power consumed by digital part = **3.9 mw**
Therefore, total power consumed = **26.13 mW**

4.9 Area analysis

	W	**L**	**Area**
M_1	1.5 μm	45 nm	67500 nm^2
M_2	1.5 μm	45 nm	67500 nm^2
M_{B4}	1.61 μm	120 nm	193200 nm^2
M_{B2}	2.24 μm	170 nm	380800 nm^2

Table 14: Dimensions of Analog part in Unit Cell

	W	L	Area
M_p	200 nm	45 nm	9000 nm^2
M_n	120 nm	45 nm	9000 nm^2

Table 15: Dimensions of Inverter

	W	L	Area
M_p	545 nm	45 nm	24525 nm^2
M_n	325 nm	45 nm	14625 nm^2

Table 16: Dimensions of Scaled Inverter

	W	L	Area
M_p	180 nm	110 nm	19800 nm^2
M_n	120 nm	110 nm	13200 nm^2

Table 17: Dimensions of Pass Transistor

	W	L	Area
M_1	1.5 μm	45 nm	67500 nm^2
M_2	1.5 μm	45 nm	67500 nm^2

Table 18: Dimensions of Sampling Switch

Total Analog Area per unit cell

$$= 67500 \times 2 + 193200 + 380800 = 0.709 \mu m^2$$

Total Analog Area

$$= 0.709 \times 255 = \mathbf{180.795\ \mu m^2}$$

Total Digital Area per unit cell

$= 9000 \times 2 + 19800 + 13200 + 67500 \times 2 + (9000 \times 2 + 24525 + 14625) \times 2 = 0.3003\ \mu m^2$

Total Digital Area

$$= 0.3003 \times 255 = \mathbf{76.5765\ \mu m^2}$$

Total Area (Digital + Analog) = $\mathbf{257.3715\ \mu m^2}$

4.10 Possible improvements

To improve the static and dynamic performance we can do the following:

1. Use segmentation to reduce dynamic errors which occur during the transitions of significant bits

2. Use larger sampling switches for quick transitions to ensure that current source transistors never enter in triode or subthreshold region

3. Calibrate the current sources to minimize the effect of mismatch

5 Self-calibration technique for improving DAC linearity

For this part, I have attempted to implement some ideas from the following paper:

D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer and C. A. A. Bastiaansen, "**A self-calibration technique for monolithic high-resolution D/A converters**," in IEEE Journal of Solid-State Circuits, vol. 24, no. 6, pp. 1517-1522, Dec. 1989, doi: 10.1109/4.44987.

5.1 Overview of the paper

Key problem addressed:
The linearity of any current steering DAC is limited by the matching of the I_{lsb} current sources. As we try to implement higher resolution DACs say upto 16-bits, limiting the standard deviation to less than half LSB becomes almost impossible. Therefore, additional calibration techniques are normally used to achieve this high resolution. The previous calibration techniques have the following drawbacks:

1. Most of the a special calibration period. During this period, the converter cannot be used for conversion, which particularly limits the application range.

2. A relatively large chip area is needed to store the error signals.

3. Techniques like laser trimming and external adjustment take precious time and facilities and are sensitive to aging and temperature.

4. Techniques like dynamic element matching need external components.

Proposed solution:
In the paper, the authors proposed a self-calibration technique which needs no calibration period, additional trimming, or external components, and is insensitive to process variations. The basic idea can be summarized as follows:

1. A single reference current source is used to calibrate all tail current sources sequentially, in continuous rotation.

2. The calibration of a single current source is based upon charge storage on the gate-source capacitance of CMOS transistors (current copier principle).

3. Whenever a current source is being calibrated, the respective DAC unit gets connected to a spare calibrated current source. This ensures that the DAC is always operational.

The circuit diagrams from the paper give us better insights.

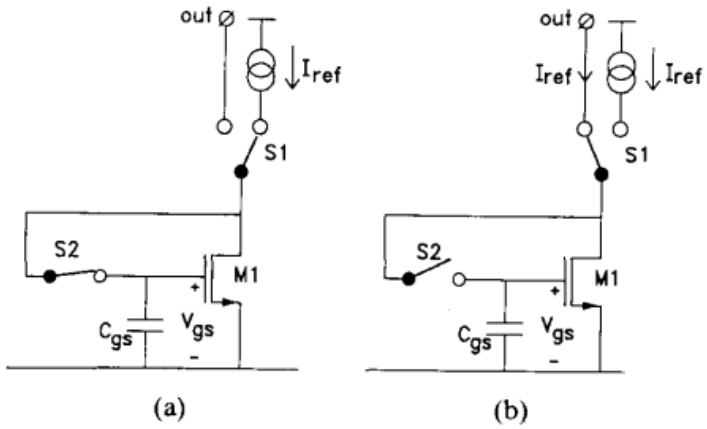


Figure 32: Calibration principle. (a) Calibration. (b) Operation

During calibration phase, I_{ref} flows through M_1 and sets the voltage V_{gs}. During operation, assuming that the charge leakage on C_{gs} is slow, a constant current I_{ref} is pulled from output due to fixed V_{gs}. By the time there is significant charge leakage, the current source is again calibrated and delivers I_{ref} output. This cycle continues.

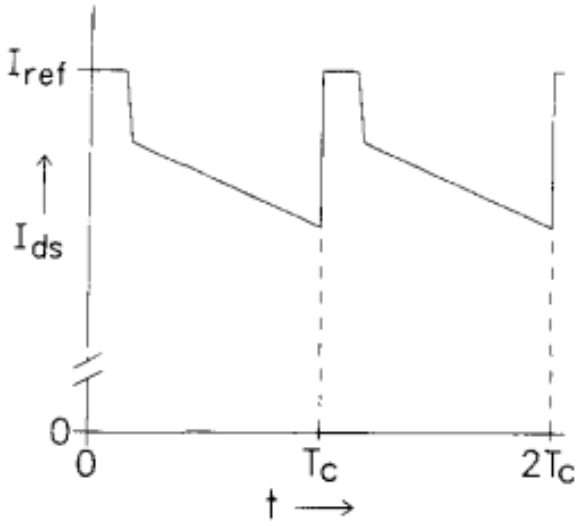


Figure 33: Drain current I_{ds} of M_1 versus time

From figure 33 we observe 2 things:

1. There is a sudden drop in current immediately after calibration. This is due to charge injection from switching transistor. The value of this drop is
$$I_{ds,q} = I_{ref} - \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}}.\frac{\Delta q}{L}\sqrt{\frac{I_{ds}}{WL}}$$

2. There is slow decay of current is due to leakage through reverse biased diode between source and substrate of S_2. The function with respect to time for this current leakage is
$$I_{ds,leak}(t) = I_{ref} - \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}}.\frac{1}{L}\sqrt{\frac{I_{ds}}{WL}}I_{leak}t$$

Based on the above results, the authors proposed an improvement to the calibration circuit - adding a mirror based current source in parallel to transistor M_1 so that current is distributed in the 2 paths and size of M_1 can be optimized to reduce $I_{ds,q}$ and $I_{ds,leak}$.

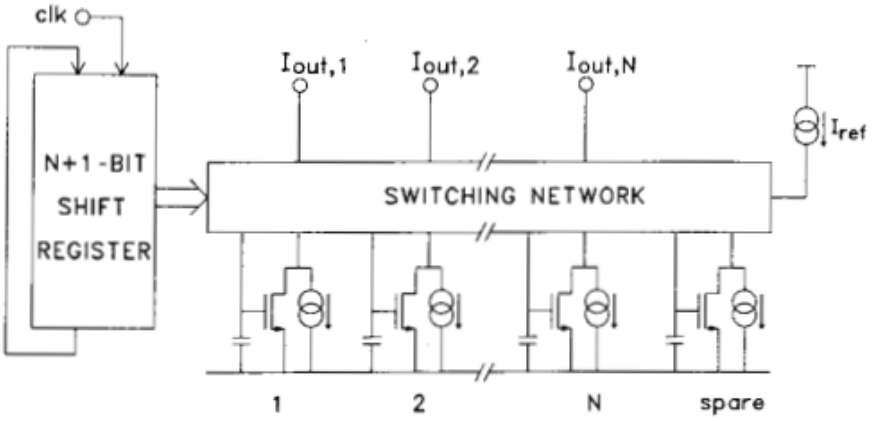


Figure 34: Block diagram for the generation of N equal continuously flowing currents.

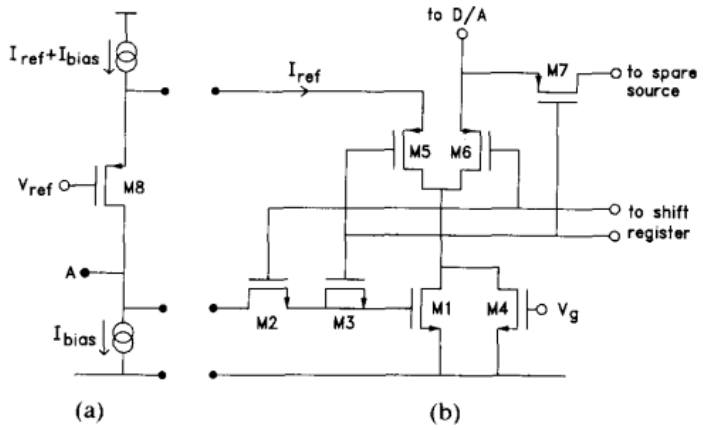


Figure 35: (a) Calibration circuitry. (b) Current cell.

Their implementation calibration circuit and unit cell is aimed at a different architecture of current steering DAC, however the key ideas mentioned above can be implemented in our project.

5.2 Circuit implementation of self-calibration technique

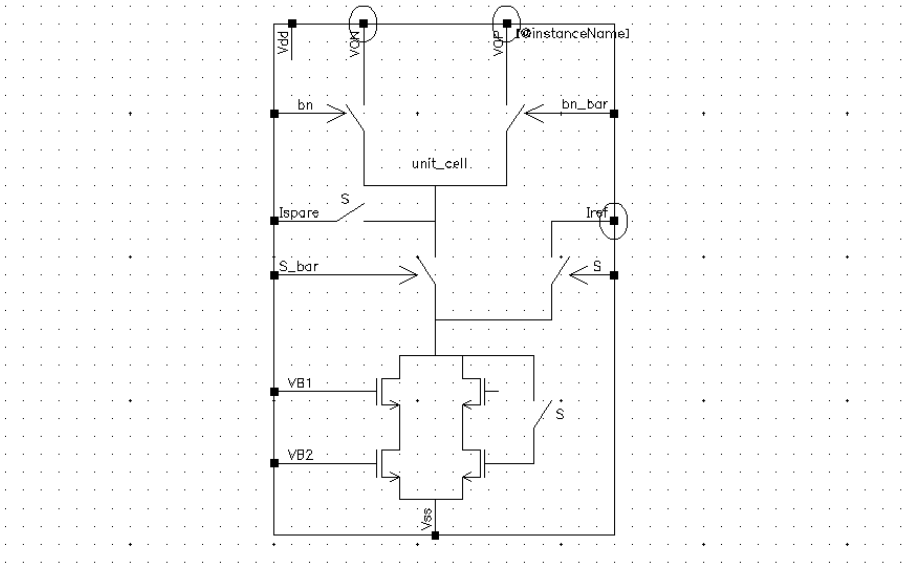


Figure 36: DAC unit cell symbol

It is important to use cascode current source like before to maintain high output impedance, otherwise this technique would not yield any benefit. However, using cascode configuration comes at the cost of headroom. To address this, I have used complementary switches everywhere and kept the drop across switches less than 50 mV (earlier it was 100 mV). Dummy switch compensation was used to minimize charge injection during switching.

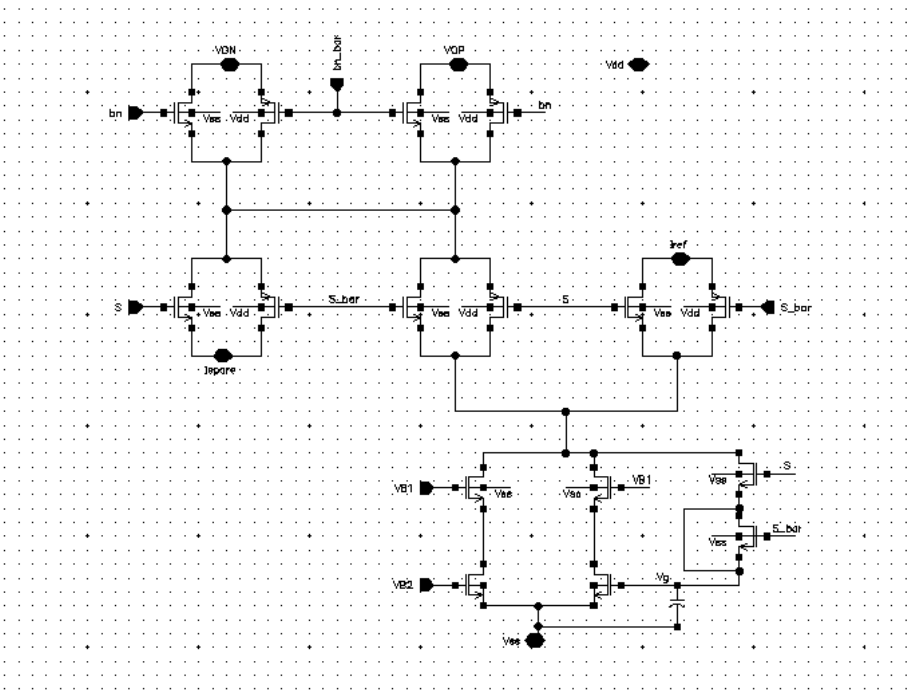


Figure 37: DAC unit cell schematic

The digital driving circuitry for unit cell was kept same as before.

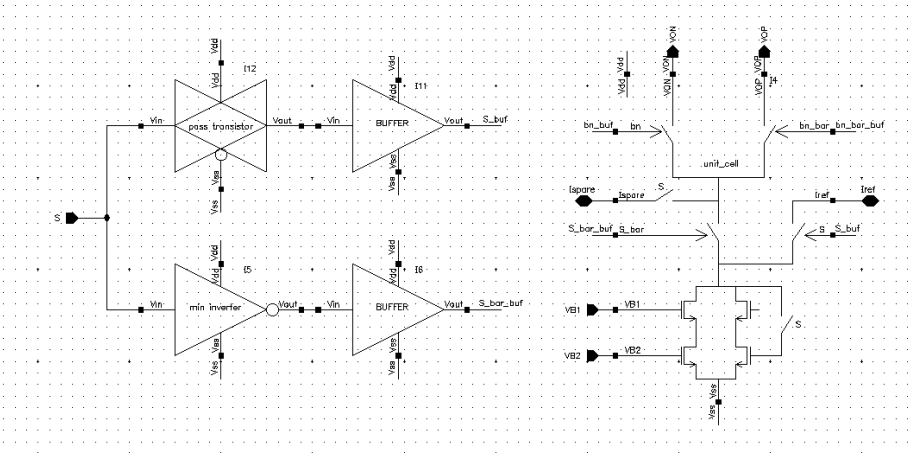


Figure 38: DAC unit cell with digital driving circuitry (1)

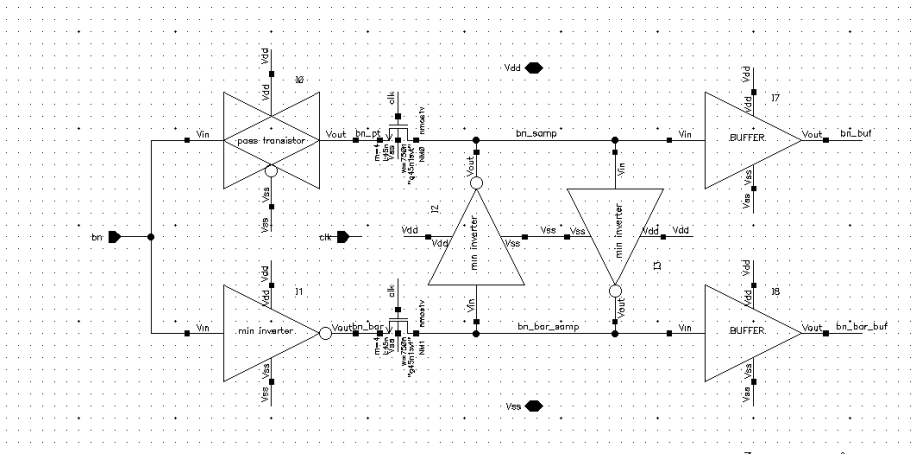


Figure 39: DAC unit cell with digital driving circuitry (2)

For shift register, verilogA blocks were implemented.

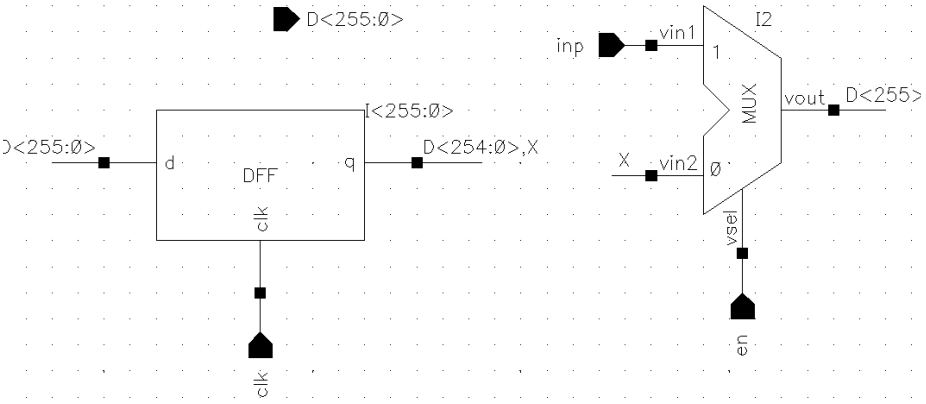


Figure 40: Shift register connected in a ring

Switch array was implemented at transistor level.

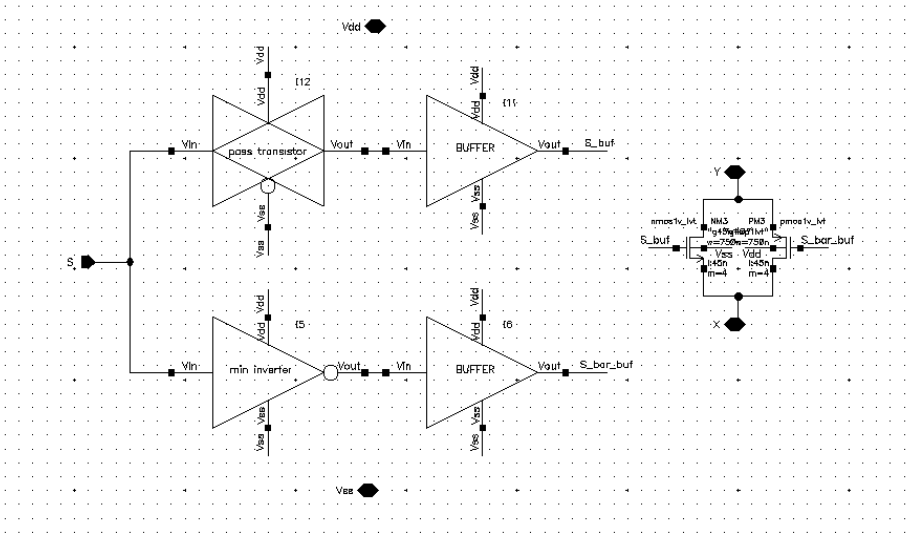


Figure 41: Switch schematic

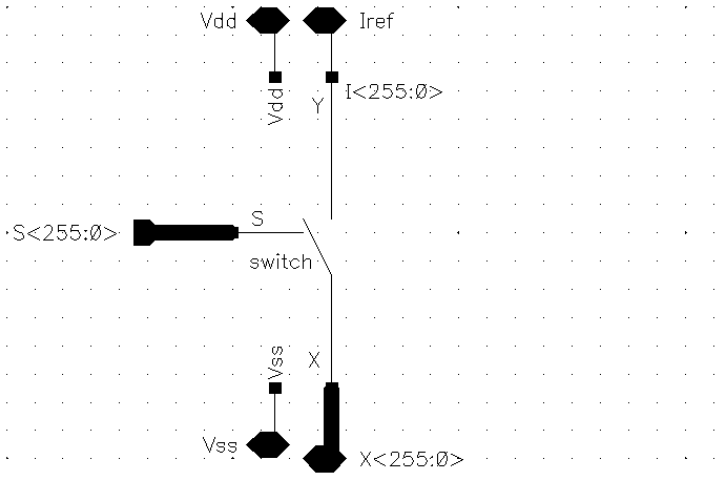


Figure 42: Switch array

Finally all blocks were connected properly to build the 8-bit DAC.

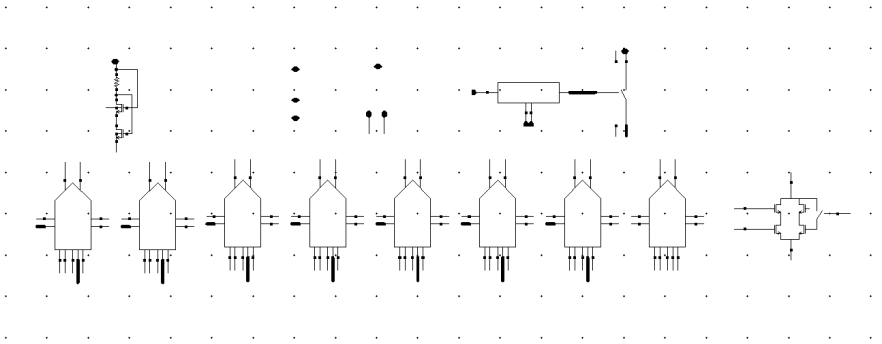


Figure 43: 8-bit DAC full schematic view

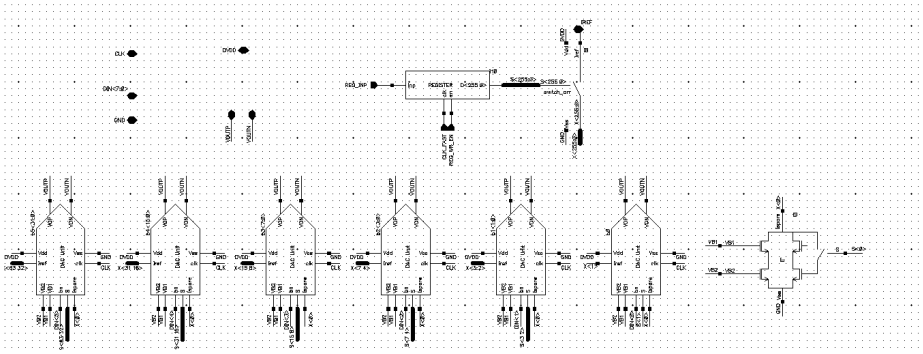


Figure 44: 8-bit DAC zoomed in view (1)

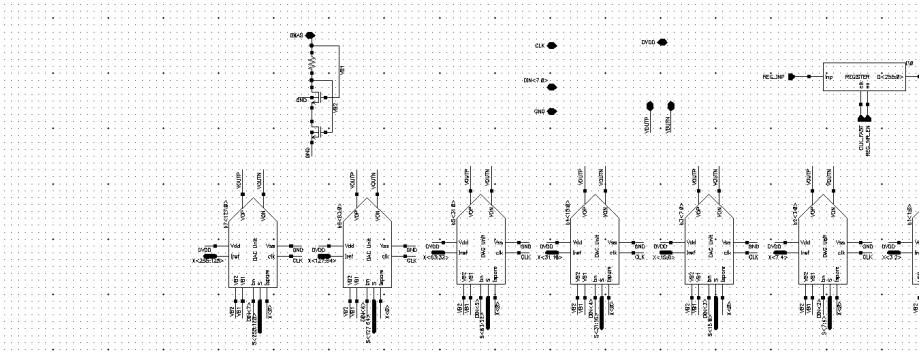


Figure 45: 8-bit DAC zoomed in view (2)

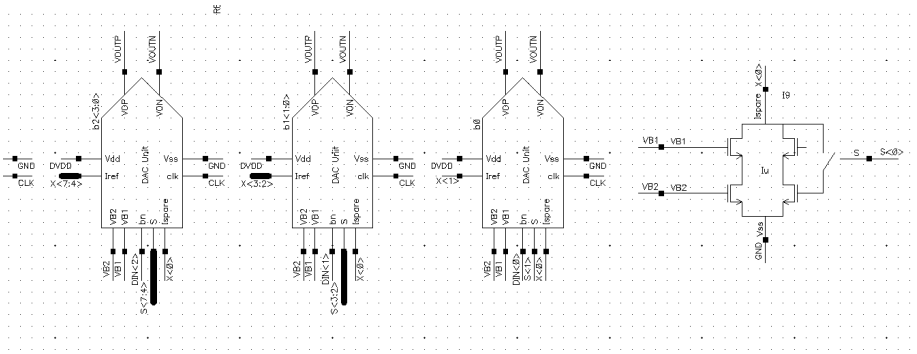


Figure 46: 8-bit DAC zoomed in view (3)

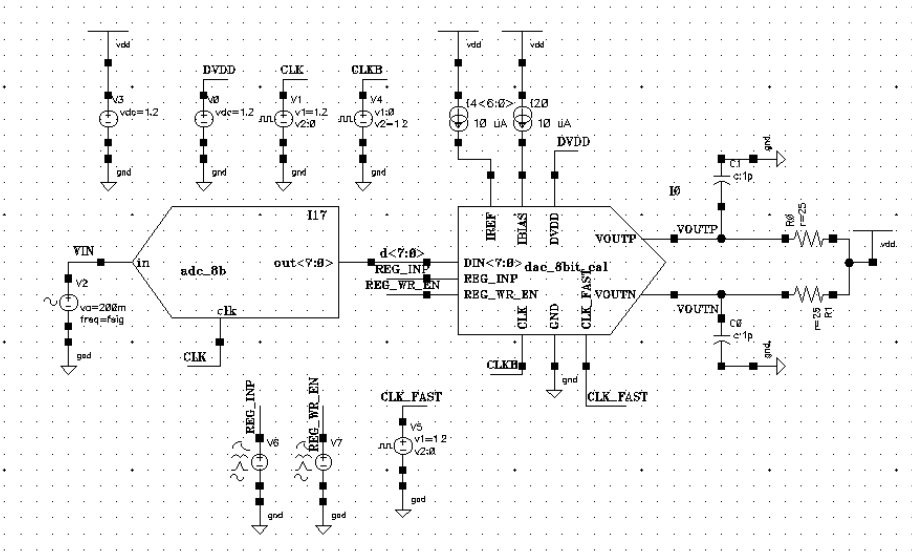


Figure 47: 8-bit DAC testbench

5.3 Simulation results

Before simulating the entire DAC, a small testbench was designed with just 2 current sources as shown. The calibration and operation phases keep toggling between the between actual DAC current source and spare source, so the DAC unit is always operational.

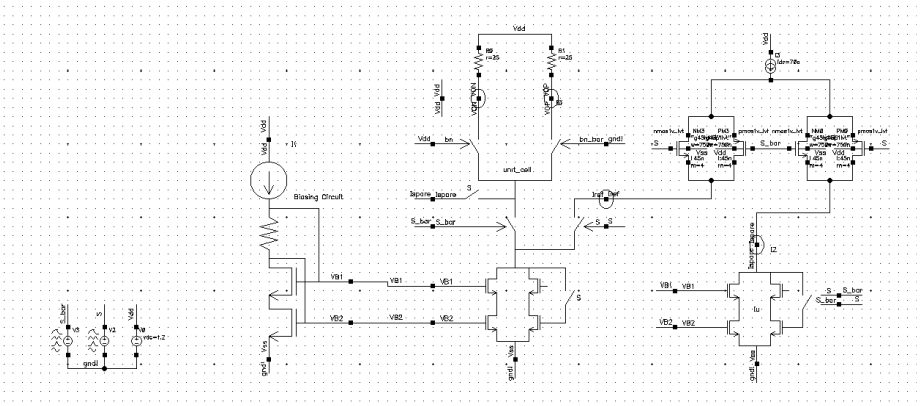


Figure 48: Simple testbench to check self-calibration

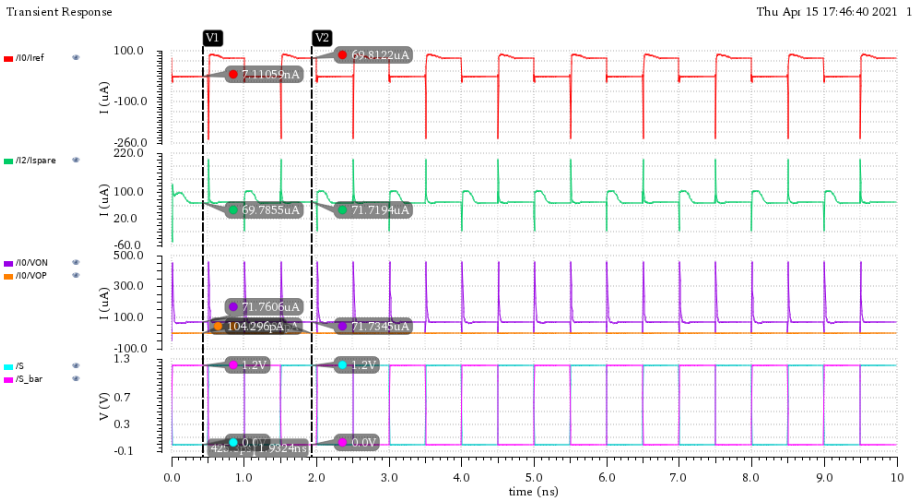


Figure 49: Transient analysis results for the above testbench

Observe that the current remains almost constant between the 2 phases and the DAC unit is always operational.

Transient simulation for the complete DAC with self calibrating circuit implementation was taking way too much time (mainly because a faster clock is required for shift registered so simulation step size is reduced). The following plots are from whatever simulations I was able to carry out in the limited time.

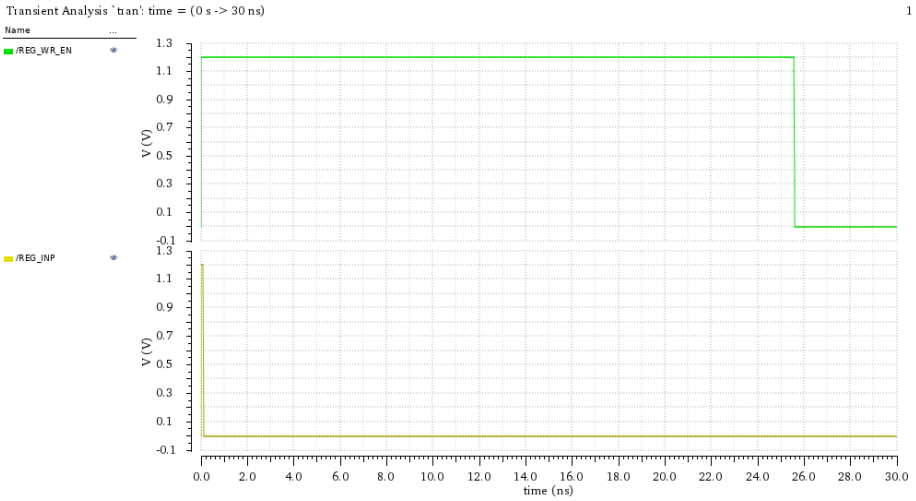


Figure 50: Shift register inputs

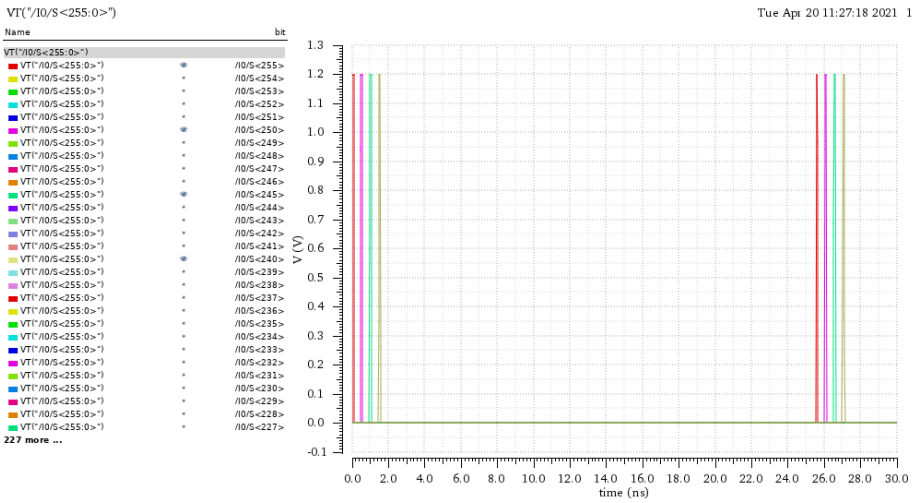


Figure 51: Sequential turning on and off of switches (only few displayed here)

It takes around 26 ns to complete one round of calibration of all current sources. After that the cycle repeats. Therefore, the results after 26 ns are of actual interest.

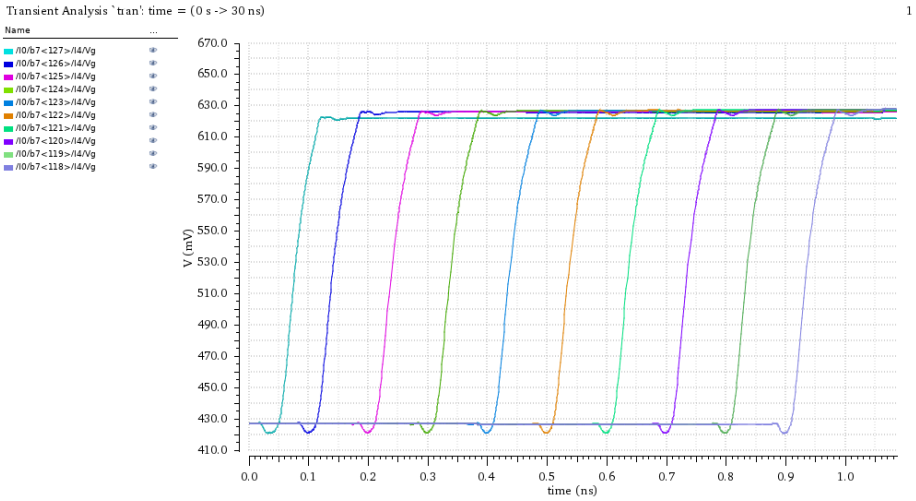


Figure 52: Gate voltages of current sources as they are calibrated for the first time

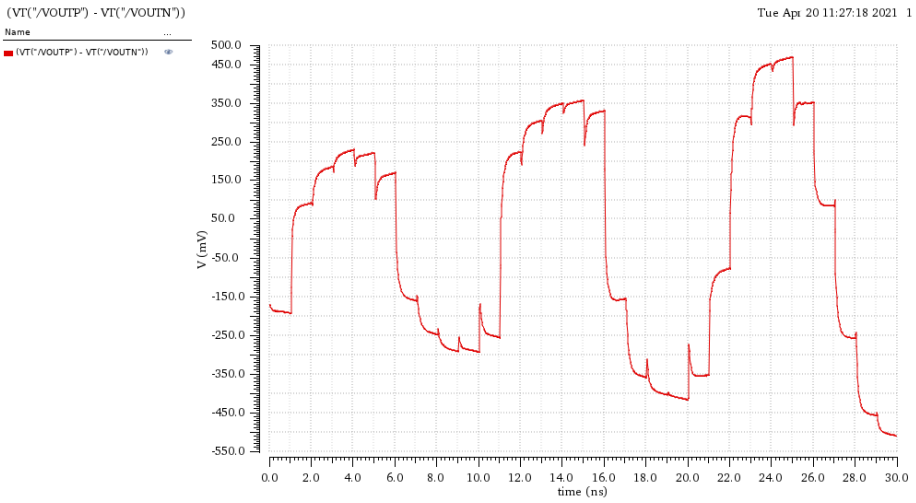


Figure 53: DAC output

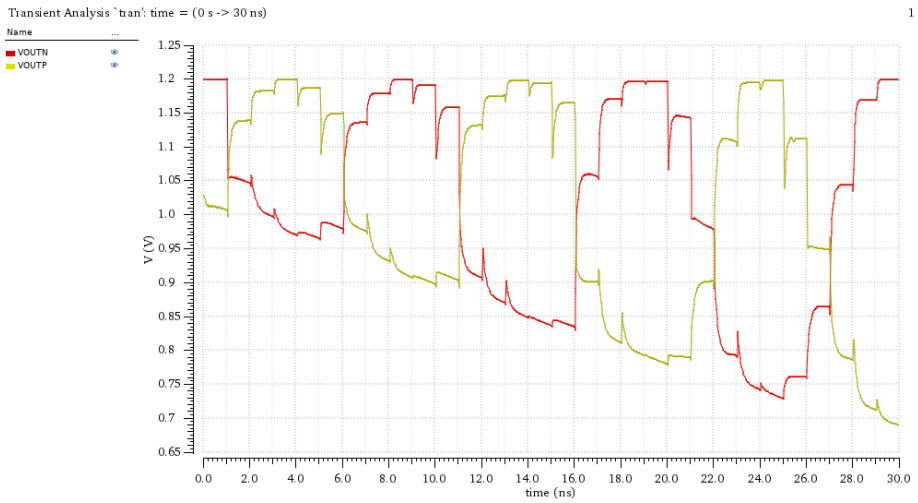


Figure 54: DAC output

There is no way to get SFDR or DNL/INL from these plots, however they at least indicate reasonably correct implementation of the idea.