EE800 Assignment 2

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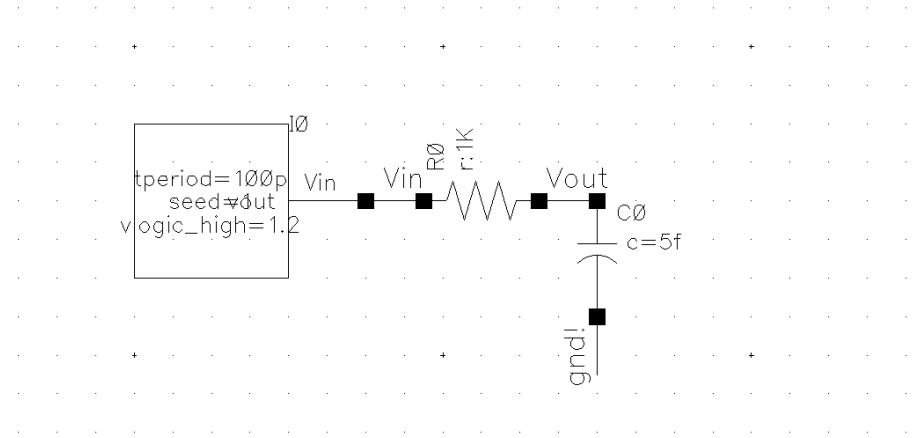

Figure 1: PRBS testbench

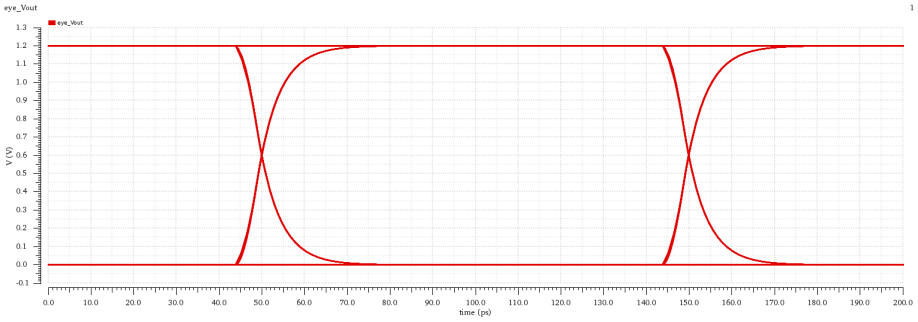

Figure 2: PRBS eye

2

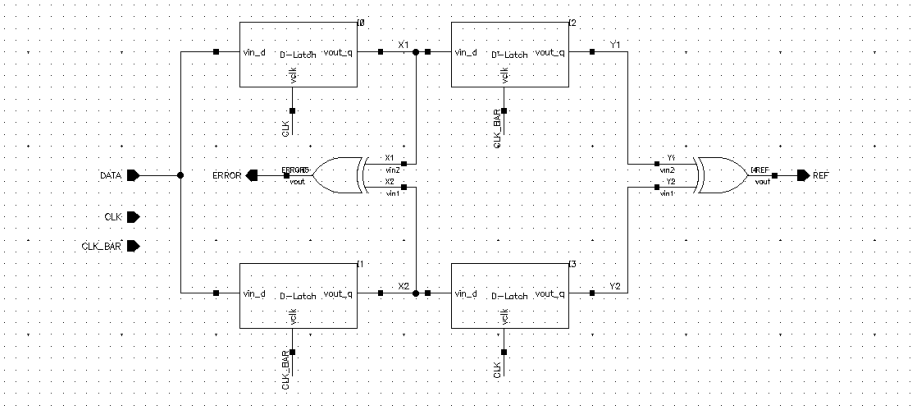

Figure 3: Linear half rate phase detector

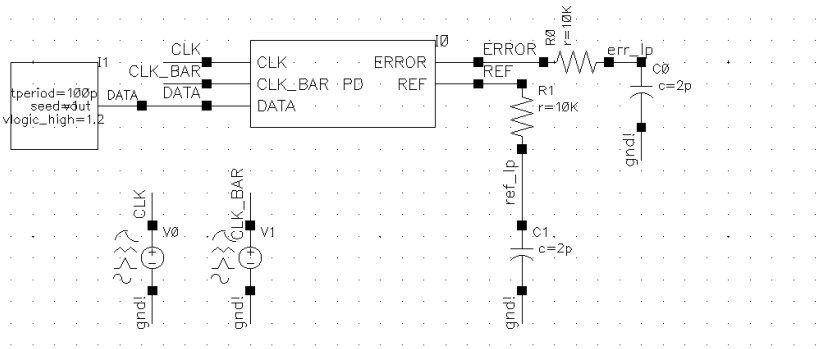

Figure 4: Phase detector testbench

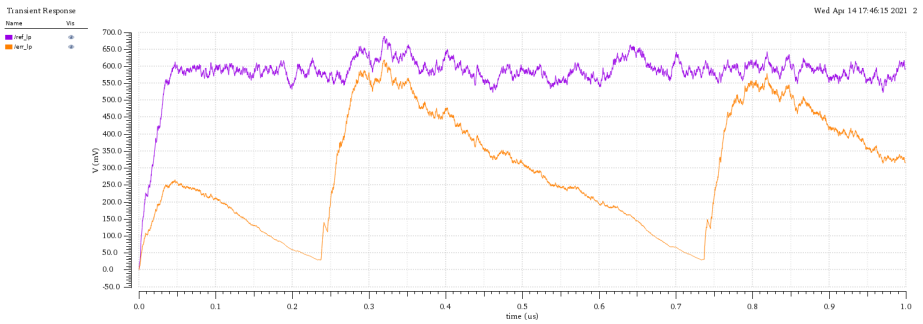

Figure 5: $V(ref\_lp)$ and $V(err\_lp)$

V(ref_lp) is low pass filtered REF output and V(err_lp) is low pass filtered ERROR output. Actual Error = Average(REF) - 2 x Average(ERROR).

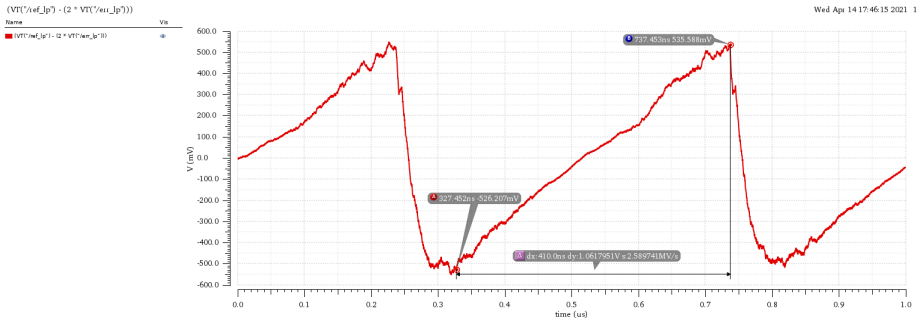

Figure 6: $V_{out} = V(ref\_lp) - 2 \times V(err\_lp)$

Slope = 2.59 MV/s . Since we are using a 5.001GHz clock with 10GHz PRBS data with half rate phase detector, in $1\mu s$ we would get 2π rad phase shift. Thus,

$$K_{PD} = \frac{2.59\ MV/s\ \times 1\ \mu s}{2\pi\ rad} = \frac{2.59}{2\pi}\ rad^{-1}$$

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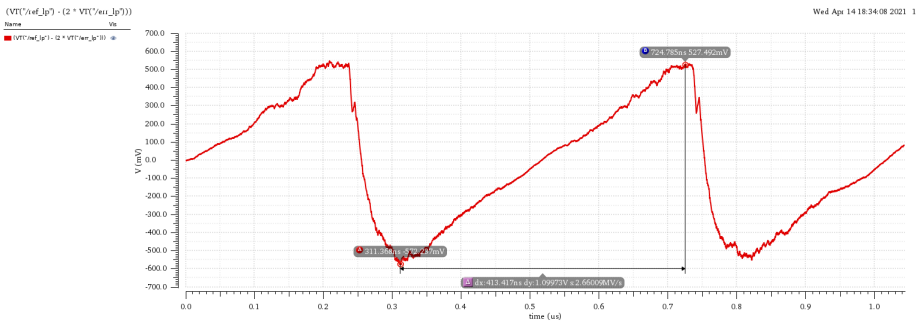

Figure 7: $V_{out} = V(ref\_lp) - 2 \times V(err\_lp)$

With realistic rise and fall times we get,

$$K_{PD} = \frac{2.66}{2\pi}\ rad^{-1}$$

The following parameters give me a phase margin of **53.1 deg**:

1. $I_{CP} = 10\ \mu A$
2. $R = 10\ k\Omega$
3. $C_1 = 5\ pF$

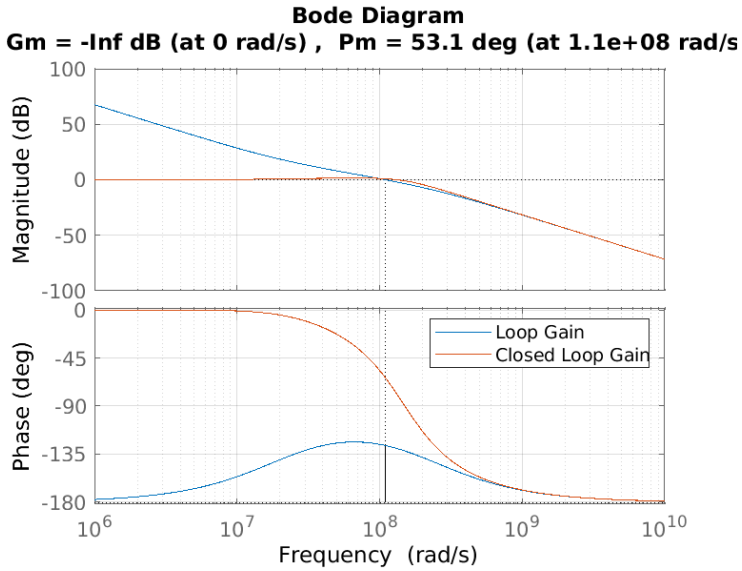

Figure 8: Bode Plot

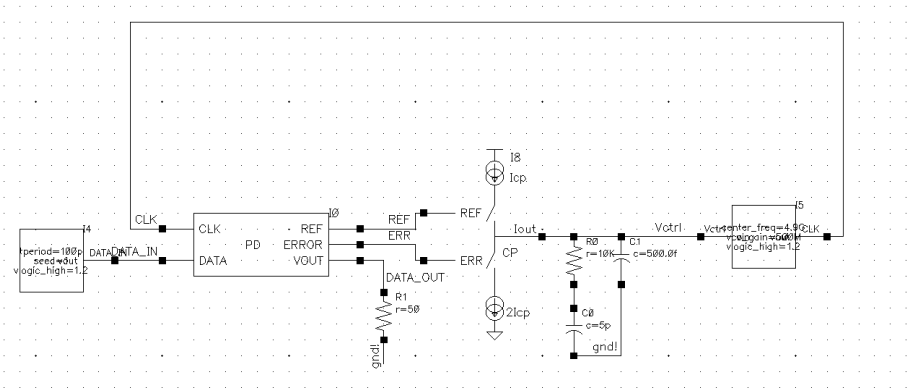

Figure 9: CDR testbench

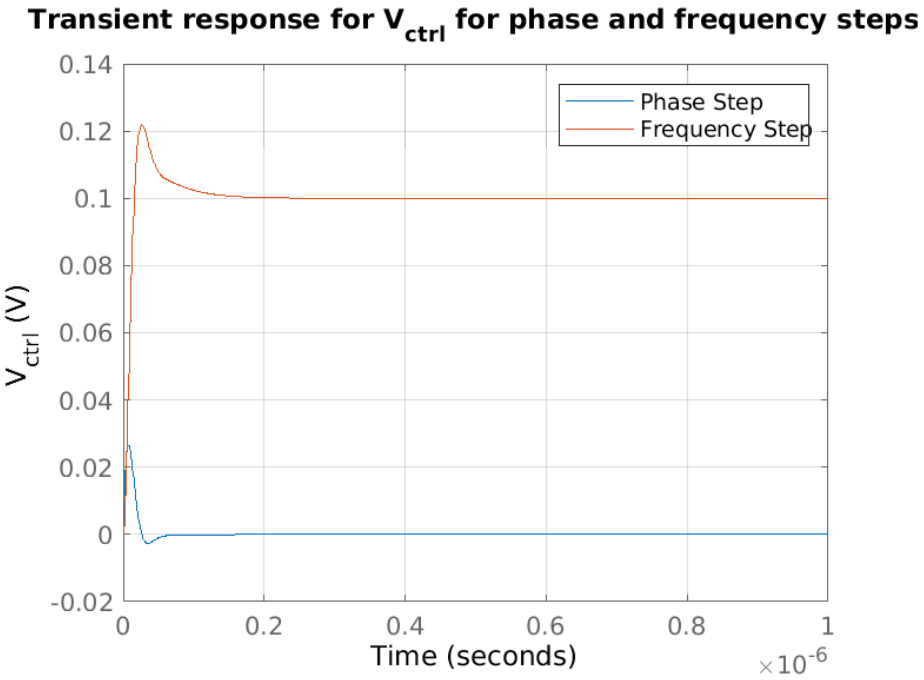

Figure 10: Control Voltage transient response obtained from MATLAB

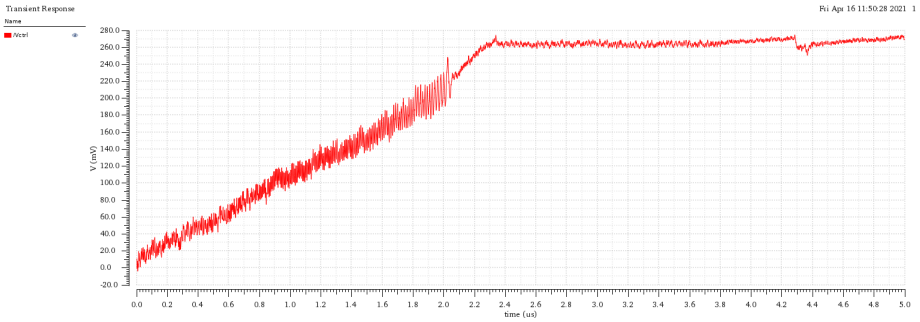

Figure 11: Control Voltage transient response obtained from Cadence

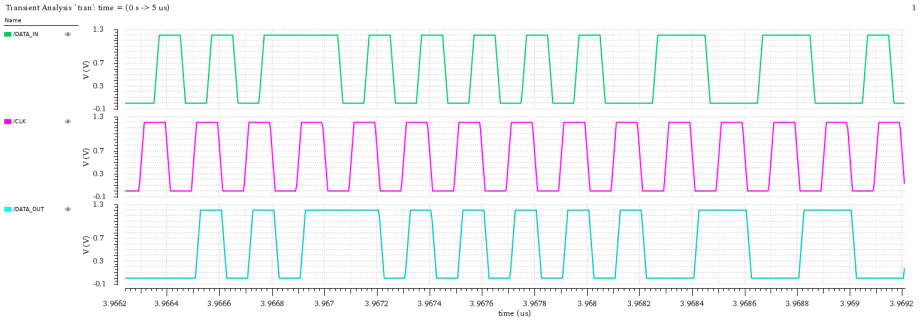

Figure 12: Transient plot of Clock, Input Data and Output Data when PLL locks

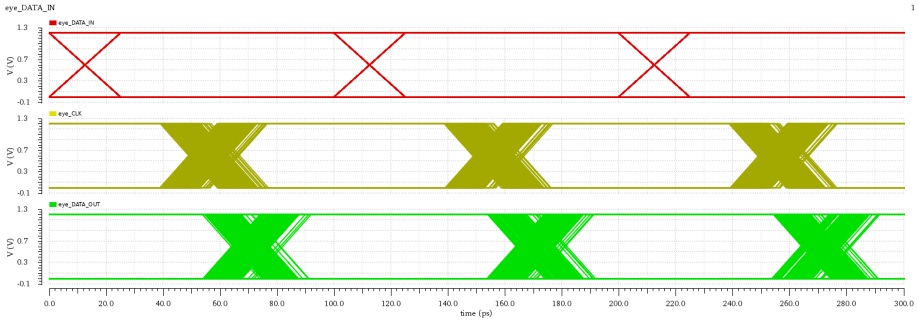

Figure 13: Eye Diagrams of Clock, Input Data and Output Data when PLL locks

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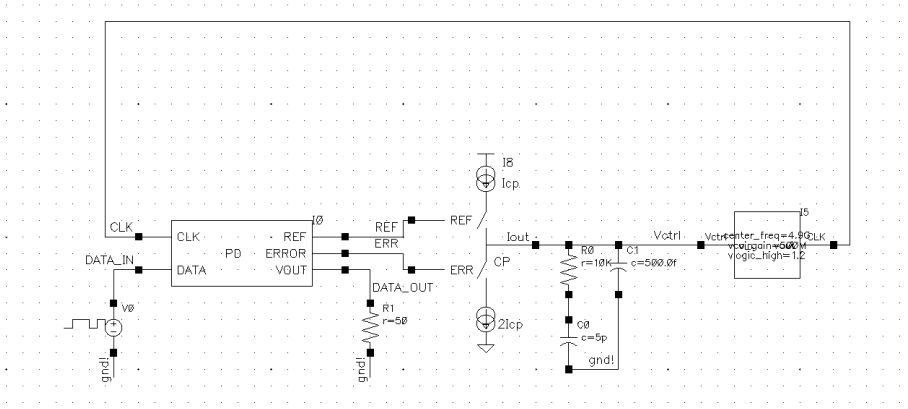

Figure 14: CDR testbench (vprbs used to add jitter)

4.1 Periodic jitter with 15 ps amplitude and 1 MHz frequency

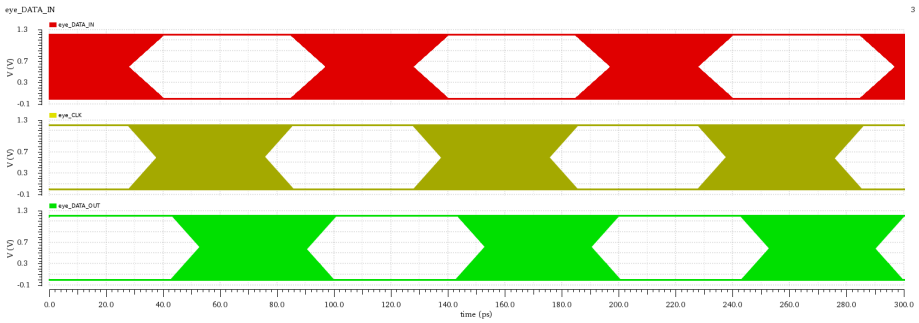

Figure 15: Eye Diagrams of Clock, Input Data and Output Data when PLL locks

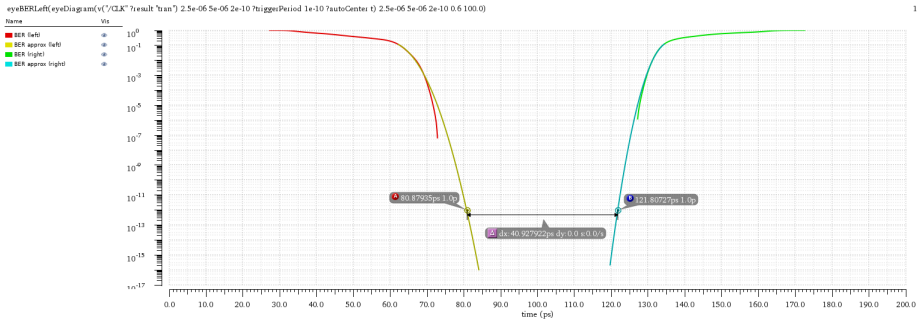

Figure 16: Bathtub curve of recovered clock

At BER of 10^{-12} the eye opening is 40.93% UI

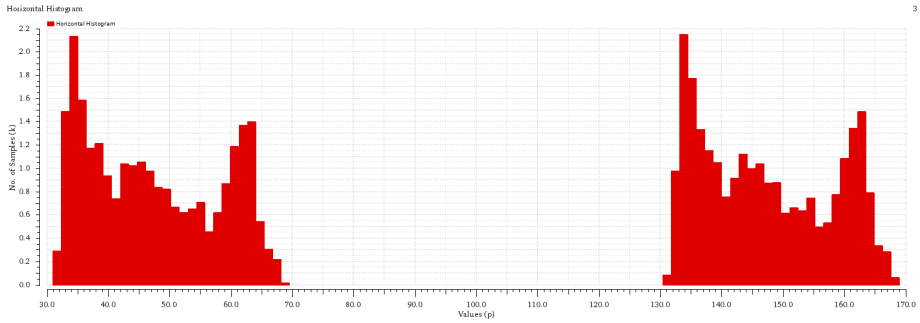

Figure 17: Histogram of recovered clock transition locations

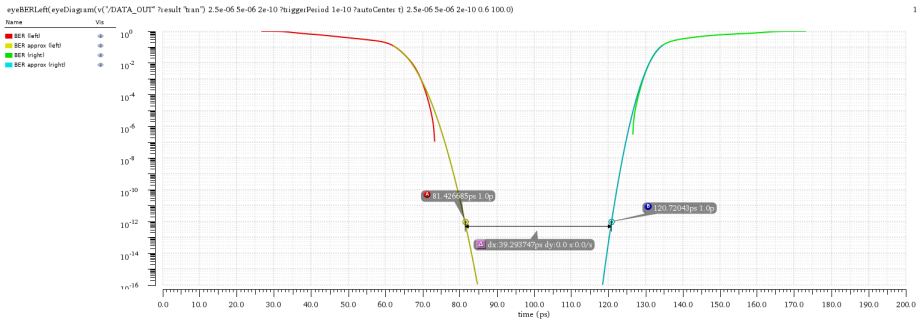

Figure 18: Bathtub curve of recovered data

At BER of 10^{-12} the eye opening is 39.29% UI

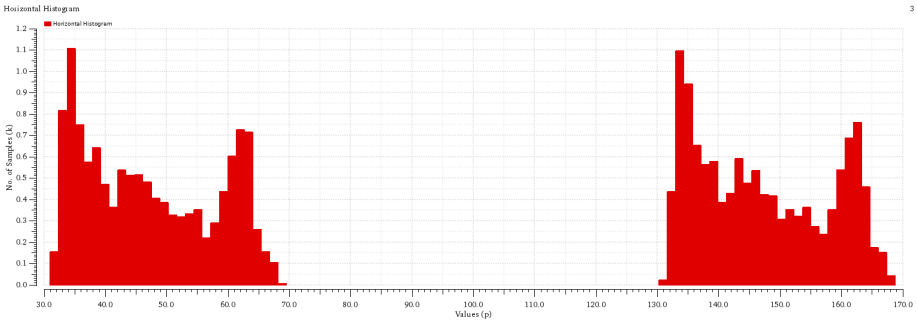

Figure 19: Histogram of recovered data transition locations

From the bathtub curves and histogram we can conclude that the clock is able to track this periodic jitter.

4.2 Periodic jitter with 5 ps amplitude and 100 MHz frequency

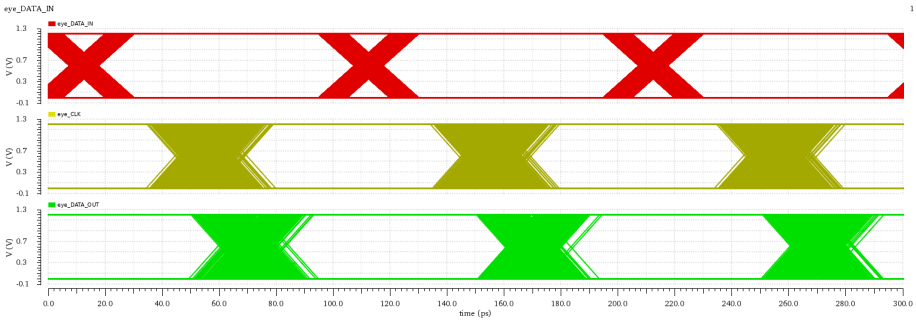

Figure 20: Eye Diagrams of Clock, Input Data and Output Data when PLL locks

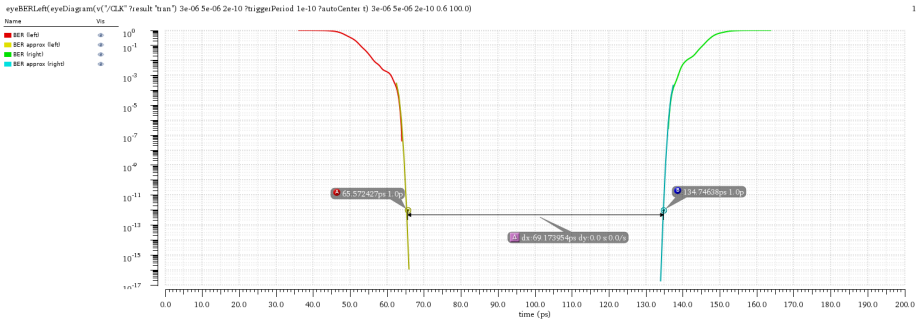

Figure 21: Bathtub curve of recovered clock

At BER of 10^{-12} the eye opening is 69.17% UI

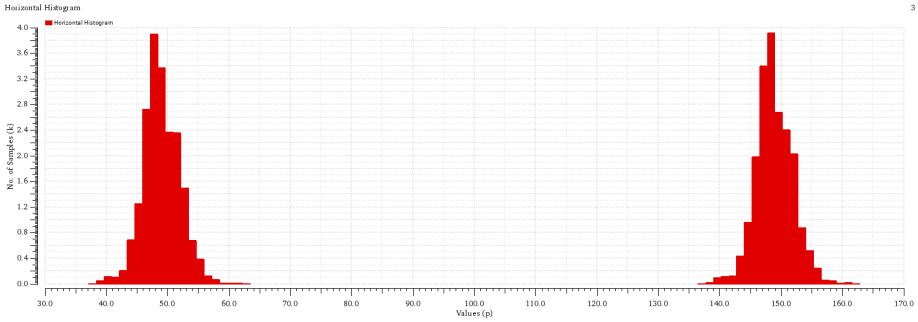

Figure 22: Histogram of recovered clock transition locations

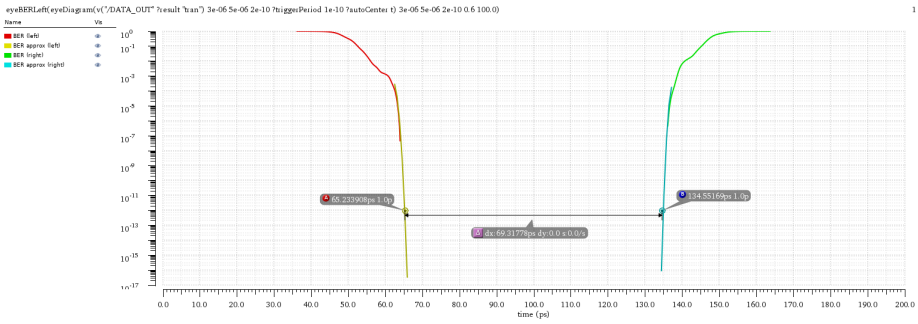

Figure 23: Bathtub curve of recovered data

At BER of 10^{-12} the eye opening is 69.32% UI

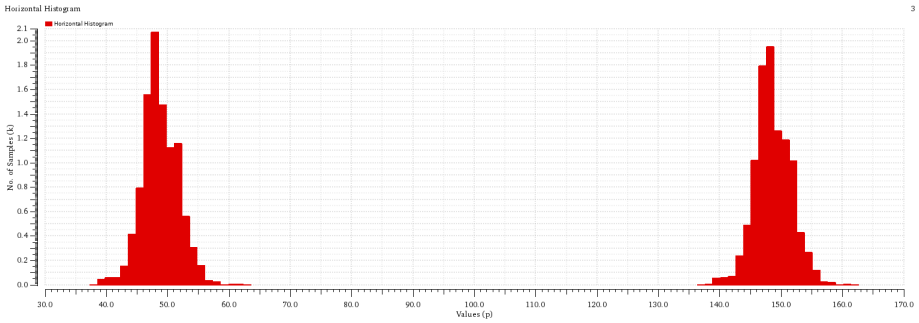

Figure 24: Histogram of recovered data transition locations

From the bathtub curves and histogram we can conclude that the clock is NOT able to track this periodic jitter. This is expected because the transfer function from Matlab analysis showed us that unity gain bandwidth of the PLL was around 16 MHz.

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With random jitter of 7 ps rms we get:

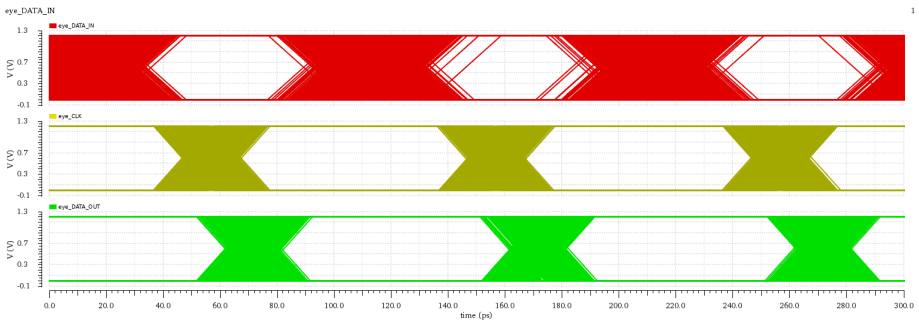

Figure 25: Eye Diagrams of Clock, Input Data and Output Data when PLL locks

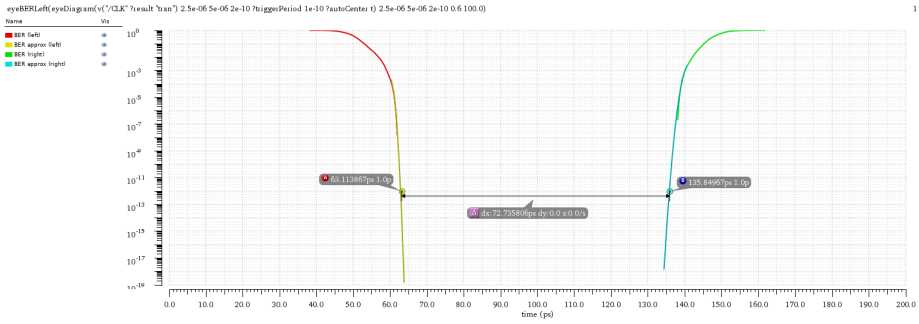

Figure 26: Bathtub curve of recovered clock

At BER of 10^{-12} the eye opening is 72.74% UI

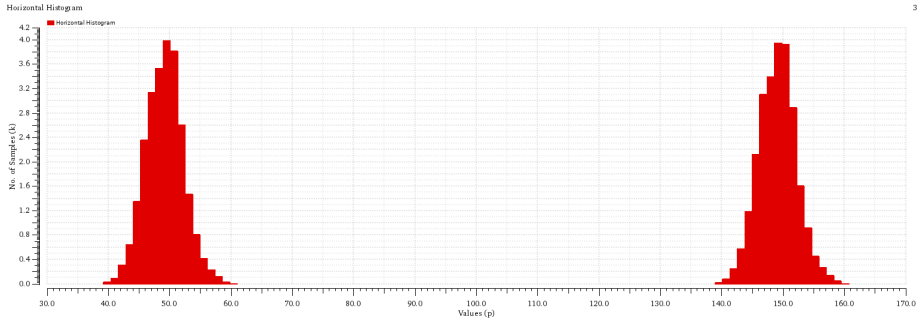

Figure 27: Histogram of recovered clock transition locations

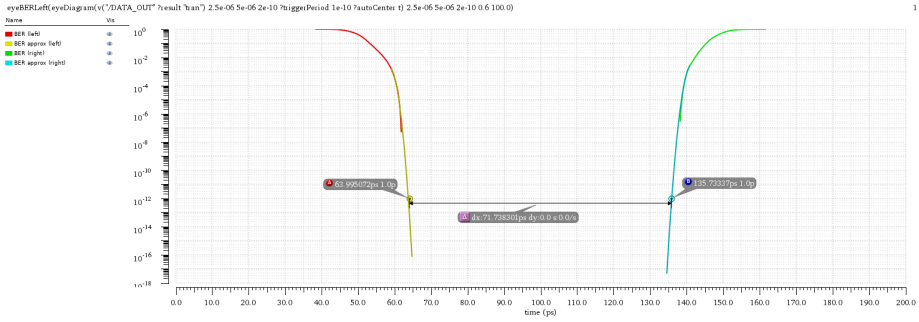

Figure 28: Bathtub curve of recovered data

At BER of 10^{-12} the eye opening is 71.74% UI

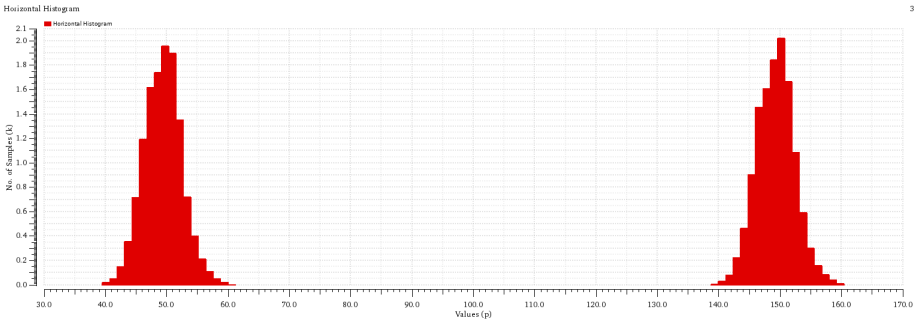

Figure 29: Histogram of recovered data transition locations