Mihir Kavishwar — Curriculum Vitae

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Research Interests

VLSI for communication systems, in-memory computing, wireless sensing, machine learning

Education

University of Illinois Urbana-Champaign, Illinois, USA [2023 - Present]
- **PhD student**, Department of Electrical and Computer Engineering
- **Advisor**: Prof. Naresh Shanbhag

Princeton University, New Jersey, USA [2022 - 2023]
- **PhD student**, Department of Electrical and Computer Engineering (dropped out)

Indian Institute of Technology Bombay, Mumbai, India [2017 - 2022]
- **Dual Degree** (B.Tech + M.Tech) in Electrical Engineering, **CPI**: 9.35 / 10
- **Specialization**: Microelectronics
- **Minor Degree**: Systems and Control Engineering

Scholastic Achievements

- Awarded **Gordon Wu Fellowship** for pursuing doctoral studies at Princeton University [2022]
- Received **Undergraduate Research Award** for exceptional work in the Dual Degree Project [2022]
- Awarded **Excellence in Teaching Assistantship** in Digital Systems course [2021]
- Secured **All India Rank 287** in JEE Advanced among 1,60,000+ candidates [2017]

Publications

1. **M. Kavishwar**, N. R. Shanbhag, "Massive MIMO Signal Detection using SRAM-based In-Memory Computing," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore.
2. **M. Kavishwar**, P. Kurrey and R. Zele, "Analog Acoustic Feature Extraction and Delta-Sigma Modulation based Neural Network Classification for Voice Activity Detection," 2022 IEEE 19th India Council International Conference (INDICON), Kochi, India, 2022, pp. 1-4, doi: 10.1109/INDICON56171.2022.10039873.
3. P. Kurrey, **M. Kavishwar** and R. Zele, "Analog/Mixed-Signal Classification for Voice Activity Detection," 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9971057.

Key Courses

Devices: Solid State Devices, Physics of MOS Transistors, VLSI Technology
Circuits: Analog, Digital, Mixed-Signal, RF, Delta-Sigma, SerDes, Neuromorphic, Photonics
Systems: Computer Architecture, Systems and ML, Sensors in Instrumentation, VLSI CAD
Algorithms: Data Structures and Algorithms, Digital Signal Processing, Pattern Recognition
Miscellaneous: Digital Communication, Random Processes, State Estimation, Optimization, Game Theory

Technical Skills

Programming: C++, Python, MATLAB, SPICE, Verilog, Verilog-AMS, SystemVerilog, VHDL
Design Tools: Cadence Virtuoso, Intel Quartus, Xilinx Vivado, KiCAD, KLayout, GTKWave

Industry Experience

System Design of PCI Express 6.0 Receiver [May'21 - July'21]
Ceremorphic India Pvt. Ltd. — Guide: Prof. Nijwm Wary, Consultant, Assistant Professor at IIT Bhubaneswar
- Proposed system architecture for PCIe6 receiver to compensate 33 dB channel loss at 16 GHz in PAM-4
- Generated an IBIS-AMI model using MATLAB SerDes toolbox and performed transient simulations
- Achieved 3.46 dB channel operating margin with statistical simulations of proposed system architecture

Verification of FPGA-based High Frequency Trading Accelerator [May'20 - July'20]
A.P.T. Portfolio Pvt. Ltd. — Guide: Mr. Vivek Panikkar, Senior Verification Engineer
- Completed training in universal verification methodology with SystemVerilog and cocotb
- Emulated MicroBlaze processor in QEMU and proposed an efficient method for verifying bare-metal code

Design and Analysis of Receiver Equalizers in High-Speed Serial Links [May'19 - July'19]
STMicroelectronics N.V. — Guide: Mr. Paras Garg, Senior Group Manager, Analog & IO Solutions
- Designed CTLE and 3-tap adaptive DFE in 32nm LP CMOS for an LVDS receiver operating at 800 Mbps
- Designed a StrongArm latch with 30 mV sensitivity to function as decision slicer at the receiver
- Successfully reduced inter-symbol interference and achieved 500 mV eye height post equalization

Positions of Responsibility

CUbiC Task Leader, PI: Prof. Shanbhag [Dec'23 - Present]
UIUC — Center for Ubiquitous Connectivity is one of the seven JUMP 2.0 research centers
- Nominated as the task leader for Programmable Energy-Efficient DSP Architectures task
- Responsible for coordinating efforts and ensuring effective communication with industry sponsors

Graduate Teaching Assistant [Jan'22 - May'22]
IIT Bombay — Course: Mixed Signal VLSI Design — Instructor: Prof. Rajesh Zele
- Assisted professor in managing logistics and course plan for a class of 70+ students
- Responsible for ideation, supervision and evaluation of course project on design of DAC with Cadence tools

Undergraduate Teaching Assistant [July'21 - Nov'21]
IIT Bombay — Course: Digital Systems — Instructor: Prof. Siddharth Tallur
- Assisted professor in managing logistics and course plan for a class of 200+ students
- Designed assignments and examinations, conducted tutorials and evaluated answer scripts

Editorial Board Member, BackgroundHum [May'21 - May'22]
IIT Bombay — BackgroundHum is the official student Newsletter of the Department of Electrical Engineering
- Lead panelist for an article covering the global chip shortage and it's impact in our department
- Lead panelist for an article demystifying the PhD program of the Department of Electrical Engineering

Institute and Department Academic Mentor [July'20 - July'21]
IIT Bombay — Student Mentorship Program enables mentorship of junior students by their seniors
- Mentored 14 undergradute freshmen by providing guidance in academic and extracurricular endeavors
- Mentored 6 sophomores in the EE department with the focus on helping academically weaker students

Extra-Curricular Activities

- Completed Lifetime Chicago Half Marathon 2023 with a race finish time of 1:57:52
- Won Bronze medal in inter-hostel Table Tennis General Championship representing Hostel 4
- Won 2nd prize in Android Hackathon organized by Web and Coding Club of IIT Bombay
- Achieved top grades in Elementary and Intermediate Drawing Examinations conducted by Gov. of Maharashtra